

May 20, 1959

MEMORANDUM TO: Mr. J. A. Harvilchuck

SUBJECT: "Get that Card-Count Down"

There are at least eight (8) ways that the card count can be reduced:

1. Use of "Dot-or" rather than emitter-follower or wherever it helps. Conversely, the use of emitter-follow or in the right places may help.

2. LOGIC SIMPLIFICATION

Boolean Algebra, Veitch charts, Karnaugh maps, flow charts, etc, can be of help. Sometimes, more logic stages permit simplification.

3. FUNCTIONAL CHANGES

The changing of functional requirements can aid in reducing count. As an example: The elimination of the A, B, P, and Q Op codes, and the change in "Transfer Program" operation permitted a reduced count.

4. MORE EFFICIENT PACKAGING

It is permissible to share cards between different logical areas on a gate.

5. TWO-INVERTER LATCH

If drive requirements permit, it may help to use the two-inverter latch in place of the CTDL latch.

6. NEW CARDS

Perhaps a change in certain of the present cards would be helpful. For instance, the elimination of a "Current Mode" output, and the addition of an extender input is required on certain cards.

7. DOUBLE CARDS

We have never really taken a good look at using a double card. It might be helpful in the MARS area, Arithmetic area, and possibly A and B registers.

8. CABLING

There may be cases where less than six wires are used in each of several ten-wire cables. Perhaps these can be combined into special cables, thereby increasing the number of spare sockets.

PCW
P. O. Underwood
Development Engineer
Dept. 280

FOU/mh

cc: W. Schaffer
P. Farbanish ←←
J. Young