JLP

February 2, 1961

MEMORANDUM TO: Mr. B. O. Evans

SUBJECT: Study of 16K-64K Storage for Stage III 1401

I Statement of the Problem

The purpose of this study was to propose and evaluate a method for expanding to 64K the maximum storage presently planned for the Reduced Cost 1401. This engineering proposal was to be evaluated by Applied Programming also to determine effects on existing and proposed 1401 programs.

To define the problem further, Messrs. J. H. Frame (Applied Programming), G. R. Ahearn and L. E. Farr (1401 Engineering), agreed that any proposal should:

1. Provide maximum compatibility with programs written for Stage II 1401 systems.
2. Include indexing facilities.

II Summary of Results

Additional Storage	Estimated Base Product Cost
16K	8,050 - 9,850
32K	14,300 - 17,400
48K	20,500 - 26,000

Costs are based on mounting additional arrays, memory circuits and power supplies in a separate frame.

By way of comparison, the difference in product cost between a 1401 Model 3 (4K storage) and a Model 6 (16K storage) is $4,851 with a corresponding rental difference of $1,650.

A rough estimate by Marketing indicates that there might be a demand for 35 to 60 systems with more than 16K of storage.

Schedules would be extended an estimated 6 months should this proposal be incorporated in the present development program for the Stage III 1401. Additional manpower would be required also (estimate minimum need for three engineers and two technicians for 6 months).

III Logic Approach

1. General Description

The existing address structure has the capacity for 64,000 combinations if the index tag bits are carried in another character. This means the A, B and C zone bits would be carried over the tens digit to expand beyond 16,000 characters to 64,000 characters. A fourth character must be added to any address to provide for the index tag bits. Incidently, this fourth character should appear as a blank in the event any system does not have indexing.

The system with 64,000 characters of storage will be capable of running programs with either 3 character or 4 character addresses. It would be required that the type of program to be run, be indicated by some preliminary steps in the load routine. In addition, it would be possible to change program mode during the operation by way of a special instruction. This feature would allow a customer to intermix 3 character mode sub-routines within the main 4 character mode program.

Now that an entire character is allocated to the index tag, it is certainly possible to have more than 3 index register words.

2. Detailed Description

The Address Register section must be expanded to handle 3 additional bits in each of the 4 registers. In a Multiply Divide system the A auxiliary register and the B auxiliary register would each require the 3 additional bits.

The Instruction Ring must have the ability to expand two extra positions. This expansion is a function of the type program and is controlled accordingly.

The Program Mode Latch would indicate the 4 character program if it were set, and the 3 character program if it were reset. Provision is made to set the latch by way of a Unit Op code followed by a modifier, or by way of a manual pushbutton.

Provision to reset the latch would be by way of a Unit Op code with another modifier, by a pushbutton or by the load key. Note that when programs enter the machine as a result of load key, the Program Mode Latch would prepare the system for 3 character programs. Therefore, the beginning of all programs must be 3 character mode. This situation is desirable because it would be a simple matter to insert a Mode Change instruction (Unit Op followed by modifier) within the 3 character section and thereby establish the controls for the 4 character material to follow.

The addressing Validity check and modifier must be expanded to accommodate the additional zone bits over the tens digit.

The circuitry in the Fixed Address Generator must expand to cover the 3 extra bits.

The following additions must be made to the indexing section if it appears on the machine:

a) Provide 3 extra lines in the path from the stars to the "A" register.

b) Provide alternate means of setting the Index tag latches under control of the Program Mode Latch.

c) Provide a conditional arithmetic cycle in the event of a carry out of the units zone bits.

The circuitry associated with the Address Modify instruction must be reworked to provide for an additional cycle in the event of a carry out of the units zone addition.

The Address Stop circuitry must be expanded to make the comparison on the 3 extra bits.

The fact that the additional circuitry is remotely located, necessitates extra signal drive blocks.

Logic has been detailed beyond that shown in the attached flow diagram to obtain approximate card counts. No detailed consideration has been given, however, to providing more index registers.

Provision to reset the latch would be by way of a Unit Op code with another modifier, by a pushbutton or by the load key. Note that when programs enter the machine as a result of load key, the Program Mode Latch would prepare the system for 3 character programs. Therefore, the beginning of all programs must be 3 character mode. This situation is desirable because it would be a simple matter to insert a Mode Change instruction (Unit Op followed by modifier) within the 3 character section and thereby establish the controls for the 4 character material to follow.

The addressing Validity check and modifier must be expanded to accommodate the additional zone bits over the tens digit.

The circuitry in the Fixed Address Generator must expand to cover the 3 extra bits.

The following additions must be made to the indexing section if it appears on the machine:

a) Provide 3 extra lines in the path from the stars to the "A" register.

b) Provide alternate means of setting the Index tag latches under control of the Program Mode Latch.

c) Provide a conditional arithmetic cycle in the event of a carry out of the units zone bits.

The circuitry associated with the Address Modify instruction must be reworked to provide for an additional cycle in the event of a carry out of the units zone addition.

The Address Stop circuitry must be expanded to make the comparison on the 3 extra bits.

The fact that the additional circuitry is remotely located, necessitates extra signal drive blocks.

Logic has been detailed beyond that shown in the attached flow diagram to obtain approximate card counts. No detailed consideration has been given, however, to providing more index registers.

IV. Storage Implementation

A. Arrays and Circuits

To provide a total of 64K of storage, 3 sections of 16K each have been assumed in addition to the basic 16K section. Each section has its own drivers and sense amplifiers. All this additional storage hardware would be in a separate frame which is tied to a system like the present 1406.

The 16K storage for Stage II 1401 systems is packaged in three sections of 4K, 8K and 4K. Each section has its own drivers and sense amplifiers. These sections will be combined into one 16K array for the Reduced Cost (Stage III) 1401. If the present driver and sense amplifier arrangement is used also, no circuit problems are foreseen. If a new X-Y driver scheme as designed by Mr. H. R. Jensen, is employed, circuit problems are unknown until a model, now under construction, is built and tested. In the latter case, the risk is felt to be reasonable in view of the potential cost savings, hence Mr. Jensen's circuits are assumed in the cost estimates of this expanded storage.

B. Hardware

The three 16K arrays and associated circuits must be mounted in a separate double frame, in a manner similar to the present 1406 attachment. Additional power supplies must be provided for these circuits and sequencing circuits to control them. Only one of the two gates for mounting chassis would be needed in this extra frame, but one intermachine power cable and one intermachine signal cable must be added to the system.

The main (CPU) frame would require modifications in several areas. The cable entry is already crowded without allowances for more storage. At the moment, this appears to be a severe physical space limitation. Modifications to the main console include additional address display and address switches. Two compatibility switches with their indicators must be added to the CE Console. Power Supply sequencing and marginal checking systems must be altered to include the additional memory supplies. It is likely that more drive will be needed to power information and address lines to the special memory frame. Finally, additional cards are required in the CPU logic (as described above) and hence, additional wiring on the chassis affected.

Product costs on all these items are tabulated in Appendex I. It may be desirable to provide two models of certain CPU chassis in order to expand CPU logic for large memory systems without adding costs to small system. Cost figures do not include amounts for this arrangement.

V Programming

Programs presently written for Stage II 1401 systems will be completely compatible with 64K memory systems. New programs must be written, of course, to utilize the added memory and these programs will contain new instructions which set and reset the address mode latch. Thus new programs provide the communication links to old programs with which they may be intermixed.

Programming costs to utilize 64K of storage, therefore, are the costs of compiling new programs specifying addresses above 16K. There would be no charges for rewriting old programs, since they would run without modifications. Costs for writing these new programs are not included in this report.

The above statements are based on the limited investigation which has been possible during the one week spent on this overall proposal for expanding Stage III 1401 storage capacity to 64K.

G. R. Ahearn

L. E. Farr

J. L. Pokoski

bd

cc: Mr. G. R. Baskin
Mr. J. H. Frame
Mr. J. A. McDonnell
Mr. F. O. Underwood

Appendix I

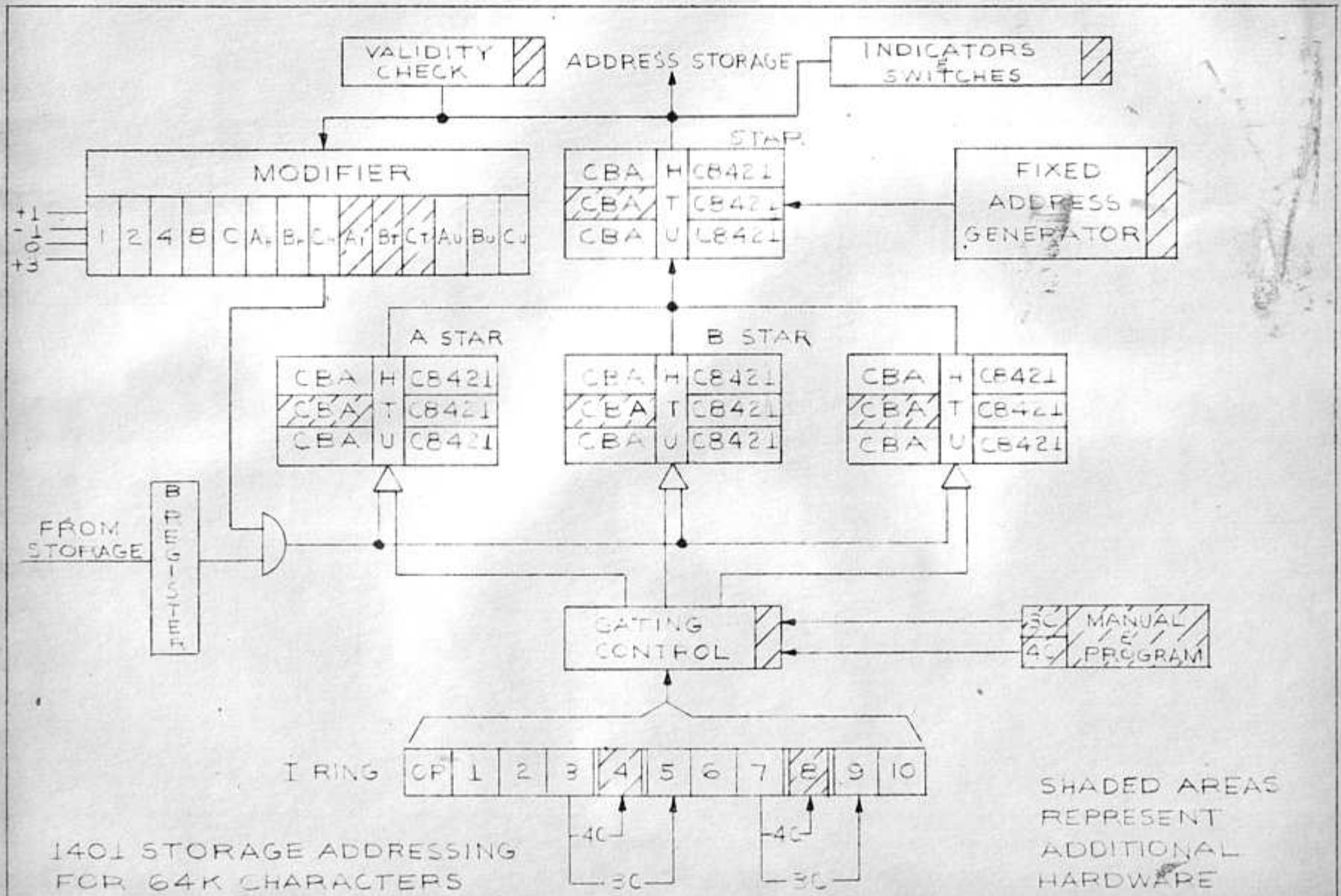
These product cost estimates are of limited accuracy. They indicate "ballpark" figures only.

Added CPU Costs

Item	Estimated Base Product Cost
Additional 16K	1,150 - 1,550
Additional 32K	1,200 - 1,600
Additional 48K	1,200 - 1,600

Additional Frame, Arrays, Power Supplies, Chassis

Additional 16K	6,900 - 8,300
Additional 32K	13,100 - 15,800
Additional 48K	19,300 - 24,400



1401 STORAGE ADDRESSING FOR 64K CHARACTERS

SHADED AREAS REPRESENT ADDITIONAL HARDWARE