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The Recording, Checking, and Printing of Logic Diagrams

M. KLOOMOK P. W. CASE H. H. GRAFF

IN THE design and development of today's complex computers, the ratio of routine and repetitive work to creative engineering is getting larger and larger. The factors which make the development of a large scale computer a lengthy and time-consuming process are more and more the sheer mass of detail work that must be performed; the drafting and checking of logic diagrams; the assignment of circuit components to printed cards, of printed cards to panels, of panels to gates and frames; the routing of signal and power wiring between the thousands of circuit components; the production of the many pieces of paper needed to convey to manufacturing, production control, cost engineering, maintenance engineering, etc., the details they require to do their work. There would be every reason to question the feasibility of embarking on a new development project were it not for the fact that a considerable number of these detail tasks are practical computer applications.

International Business Machines Corporation (IBM) is using *700* series computers (*704*, *705*) to assist in the design, development, release, and product engineering of the new *7000* series of general-purpose data-processing machines. This system of computer programs is referred to as the "Design Mechanization System." In this system the computer does not replace the design judgment and knowledge of the engineer. Its function is to eliminate the manual repetitive execution of established procedures following rules laid down by the design engineer. IBM is also using *700* series computers to assist the engineer in the design of logic. Computer assistance in logic minimization, logic implementation, logic simulation, and physical placement is the subject of future papers and is not considered here.

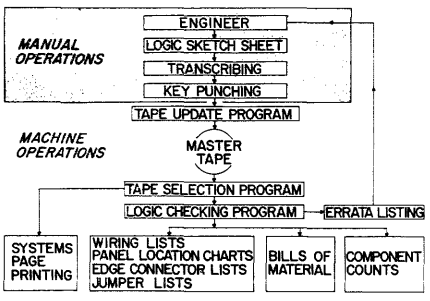

Fig. 1. Component parts of the design mechanization system

Component Parts of the Design Mechanization System

The phases of the design mechanization system discussed herein are shown in Fig. 1. The development engineer in designing computer logic presents his ideas on a system drawing. This rough sketch is then coded for key punching and punched into cards. The cards are read into the computer and the master tape is updated. The master tape contains a complete historical record of the design to date and is the source of all data for succeeding programs. The "master tape select program" selects from the master tape any desired section of the machine for further processing.

The "logic checking program" operates on a complete section of machine logic and checks for adherence to design rules. In addition to checking for proper circuit configurations, many logical checks can be made to test for redundancies and proper page-to-page notation. Most of the rules established in a given machine design program can be inserted into this process. The output, in the form of an errata list, can then be returned to the design engineer for his corrective action.

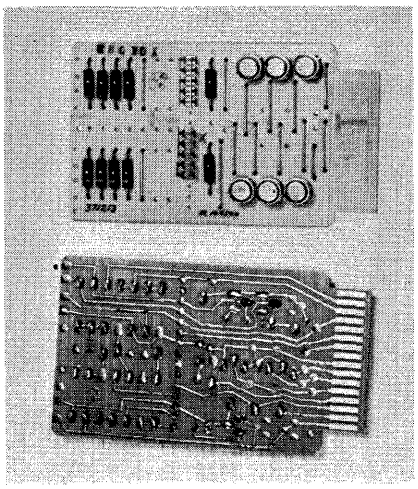

Fig. 2. Basic components of SMS, printed circuit cards

The "systems page print program" converts the coded logic record appearing on the master tape into a computer-prepared systems drawing in block diagram form. Preparing the printed logic page by machine saves large numbers of man-hours over the drafting process formerly used. Other advantages are greater speed of preparation, increased accuracy, a uniform quality of printing regardless of the number of changes to which a given page has been subjected, and the ability to recreate an old engineering level page when needed.

The "panel wiring program," operating on a section of checked logic, routes the necessary panel wires in such a fashion that lead lengths are minimized, taking into consideration capacitive loading and interwire noise. The output is a panel wiring chart to be used as a release document for construction of the panel. A secondary objective is the ability to alter previously computed panel configurations to accommodate "engineering changes," and to make updated panel wiring lists.

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The "bill of material generation program" uses the checked logic to generate bills of material for electrical components. This is merely a matter of extracting data from the master tape about the location and quantity of component circuits, and referring to tables to assemble the proper information in the desired format. This program also must provide for handling engineering changes.

The design philosophy which makes design mechanization a practical reality is the far-reaching standards program adopted at IBM. The key to this standards program is the "standard modular system" (SMS). Before going into the details of the design mechanization system it is worthwile dwelling briefly on SMS.

Standard Modular System

The standard modular system is an engineering program for uniform application of solid-state technology in a new generation of IBM data processing machines. SMS makes possible a flexible, standardized packaging system for IBM's new *7000* series transistorized computers.

The basic component of SMS is the printed circuit card shown in Fig. 2. This card is pluggable into sockets on a standard panel. The panels in turn are packaged into one of two standard modular frames. Fig. 3 shows a sliding gate that fits into the larger of these frames. Four standard panels are seen on the gate.

By selecting appropriate quantities of either of the standard frames, packaging is available for data processing equipment ranging from desk size to the giant *7000* series.

A standard range of circuits is used throughout for logical design, so that the logical design process consists of selecting pre-designed standard circuit cards to implememt the logic.

SMS and design mechanization complement each other, since standard packages make possible the use of more generalized computer-aided design techniques. These techniques in turn enable more sophisticated automated manufacturing methods to be used. In addition, the standard circuits lend themselves to computer and checking techniques.

Input

Logic Sketch Form

The input document to the design mechanization system is the logic sketch form. This form has been designed with several objectives in mind:

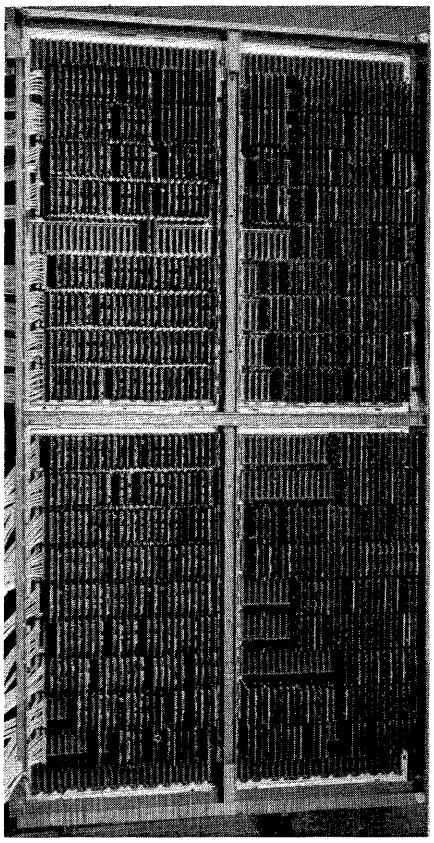

Fig. 3. SMS gate with four standard panels

1. Clarity of logic flow. The page is large enough to enable the development engineer to present a logical entity, and not so large as to appear cluttered, overcrowded, or confusing to the maintenance engineer who must service the equipment using these documents.

2. The page must be of a size to be printed by the standard IBM line printers.

3. Clarity of presentation for the non-technical people who convert the information into punched cards.

The resultant form is shown in Fig. 4(A). A maximum of 45 logic blocks are permitted, arranged in a 5×9 array. A co-ordinate grid is superimposed for ease of reference to any given circuit block. Provision is made at the top of the page for the required identifying information and at the bottom for comments. The numbers in the background indicate the number of alphanumeric characters permitted for each name. Thus, for example, each line entering or leaving the page can have an identifying name 30 characters long, expressed in two lines of 15 characters each.

The form is printed on vellum with the guiding information printed in non-reproducible blue ink. In using the form, the engineer marks in freehand the blocks he wishes to use, the lines between the blocks, and the off page lines as in Fig. 4(B). He then obtains a facsimile of the drawing for the design mechanization system, retaining the original for his own use until presented with a final drawing, prepared by the computer, see Fig. 5(A). This final drawing is also on vellum.

When a change or correction is made to any page, the computer-produced vellum is marked up as shown in Fig. 5(B) and resubmitted as an engineering change. A new computer-produced vellum master is then prepared.

Transcribing

The conversion of the information on the logic sketch forms into digital data for key punching is effected by a group of clerks called transcribers. The transcribing form is shown in Fig. 6(A). The numerical designations on the transcribing form refer to the card columns into which this information is key punched. No knowledge of circuit logic or convention is required and familiarity with the transcribing rules can be achieved by an average clerk in about one week.

Each logic sketch sheet is encoded into the transcribing form in the following sequence as in Fig. 6(B).

1. Heading Information. Space is provided at the top of the transcription sheet to record the identifying information.

2. Information in the Circuit Blocks. The fields in the body of the form are blocked out to indicate the allowable number of characters and are numbered to indicate the card columns into which the information is to be key punched.

The circuit blocks are identified by their co-ordinates on the sketch sheet and transcribed in order, from top to bottom and right to left. There are six lines of alphanumeric information inside each circuit block and the columns labelled Line 1, Line 2, . . . Line 6 on the transcribing form indicate where this information is to be written.

3. Signal Lines. After all circuit blocks are transcribed, the lines between blocks are encoded. All lines are described in consecutive columns of the transcribing sheet, and the titles have no meaning here.

All lines are considered coming from, rather than to, a block with lines entering the page on the left considered coming from a set of pseudo blocks on the left side of the page. Lines are described by their beginning and ending co-ordinates. Line routing is performed by computer.

4. Supplementary Information. Space is provided at the bottom of the transcribing form for the comments indicated on the logic sketch sheet.

The Master Tape

Master Tape Format

The heart of the design mechanization system is the master tape which contains a complete historical record, block by

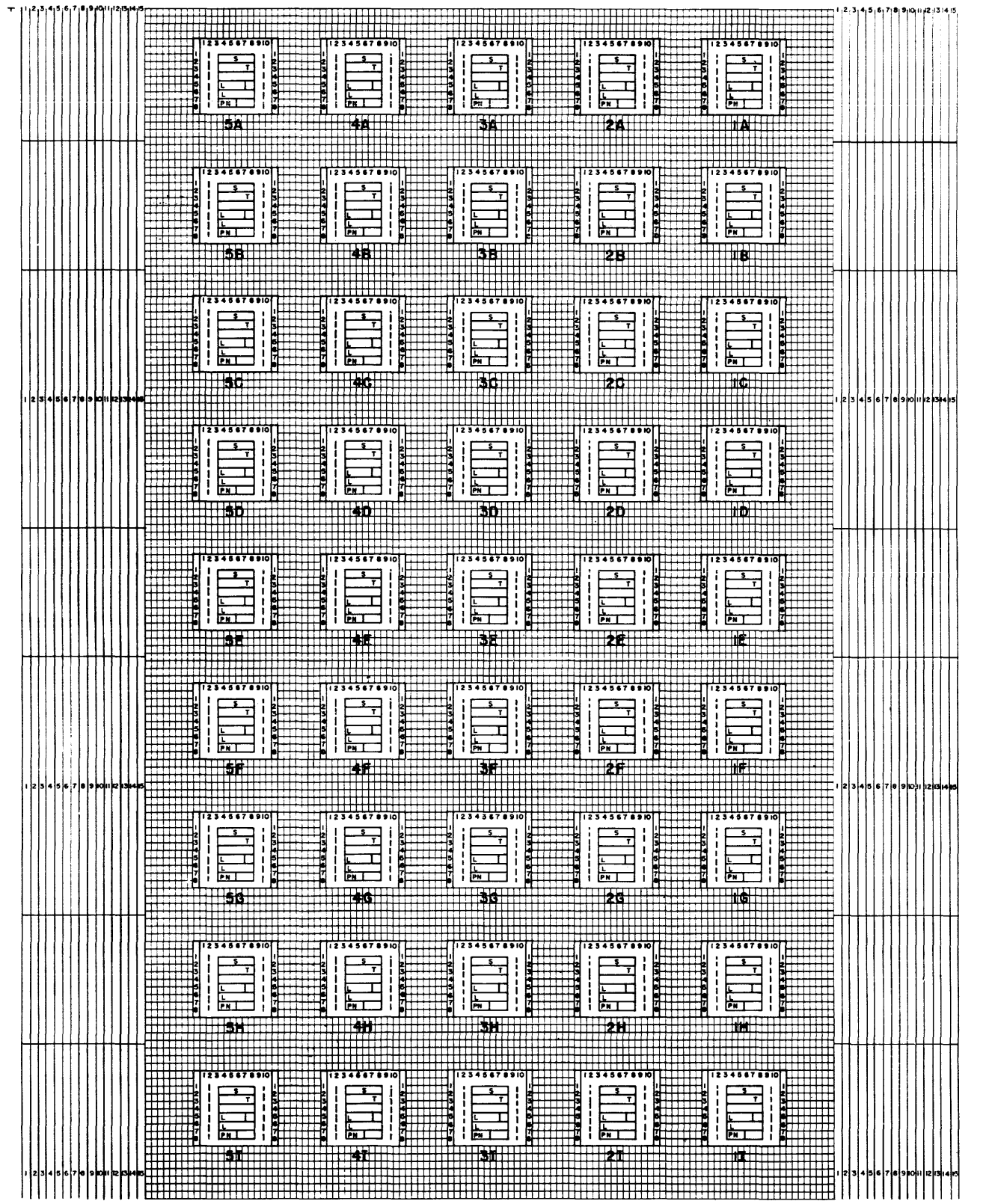

Fig. 4(A). Logic sketch sheet

block and page by page, of the machine logic. This master tape is updated periodically as necessary and is kept current from the early stages of development until the machine is serving customers in the field.

The organization of the master tape is illustrated in Fig. 7. The first record on the tape is a machine identification. Separate master tapes are kept for each machine using the Design Mechanization System. This is followed by a record for each page, including the name, part number, comments, etc. Following the page record is a separate record for each block on the page. Blocks are described in the order in which they are used on the logic sketch sheet. Only the blocks which are actually used are recorded on tape. Block information is kept in order of most recent engineering level, but information at all levels is always retained. There are two reasons for maintaining this historical information.

1. During development, an engineer at his own discretion can discard any logical design and revert to an old configuration.

2. During production there may be machines in the field at many different levels, depending on the date of manufacture or on the customer's choice of special features.

The record length for each logic block is variable, depending primarily on the number of output lines. An average block, with one output line requires 70 characters. A typical machine with 1,000 pages at a representative number of engineering levels requires about 1,200 feet of tape.

Master Tape Updating Program

Updating is performed each day, if any activity took place, by writing a new master tape, merging the information on the old tape with the cards prepared in the transcription process. During the updating run, provision is made to rearrange any section of the master tape, renumber pages, rearrange blocks, etc., at the discretion of the engineer. Of particular interest is a page rearranging routine. This routine can be run wherever it is desired to alter the arrangement of the page in the interest of clarity or appearance.

Master Tape Selection Program

During the master tape updating run, a "request card" is punched for each page affected during the run. The request card contains the page number, part number, and engineering level. A file is kept of these cards for use with the selection program which prepares a new tape of any page or section of machine at any engineering level. This selected tape is the input for the print program or the checking program or both. Provisions are made for selecting all pages at their latest engineering level, when it is desirable to avoid inserting large quantities of request cards.

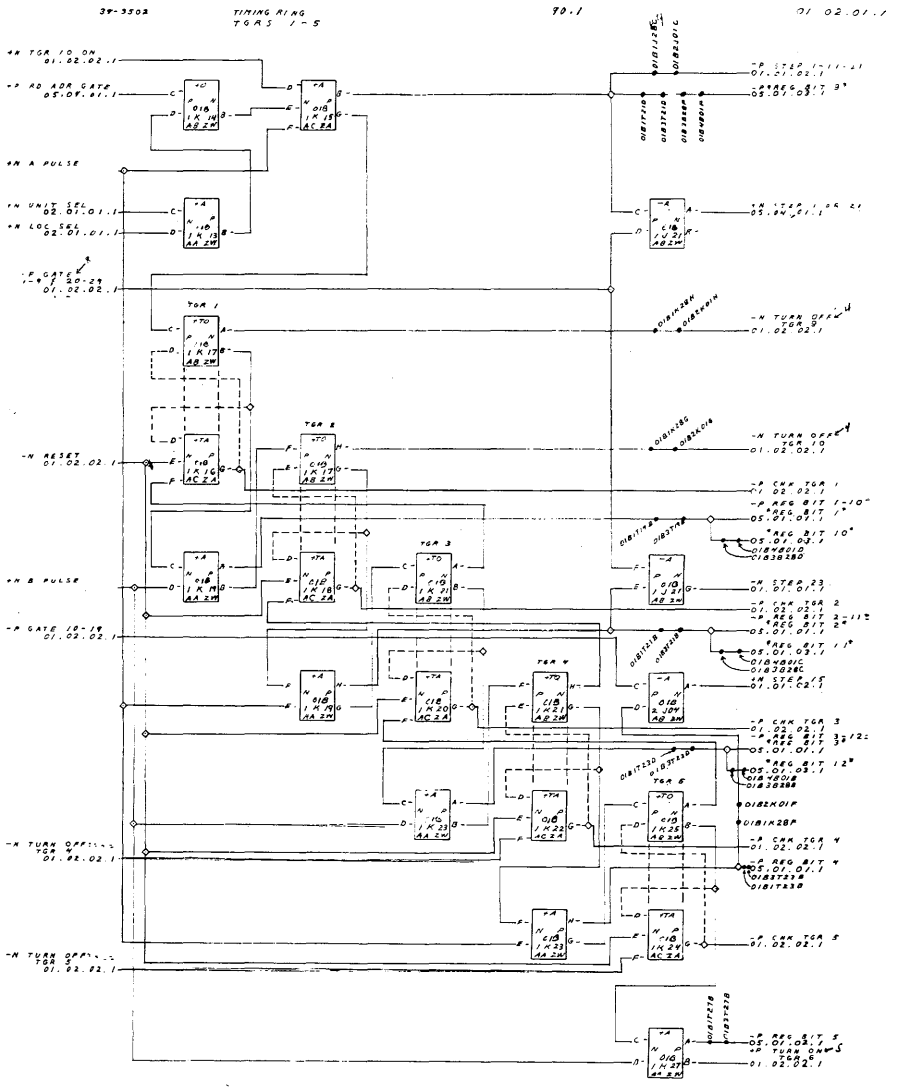

Fig. 4(B). Logic sketch sheet with typical entries by computer

Print Program

Page Size

The logic diagram shown in Figs. 5(A) and (B) was printed from tape on an IBM *717* printer. The only modification to the printer was the addition of a set of six special symbols to each type wheel.

The circuit blocks printed on the page are constant in size, 6 characters wide and 7 lines high. Two factors govern the size of the blocks; the necessity for printing all pertinent data, logical function, transistor type, physical location, circuit part number, etc. in a clear and legible format, and the desire to keep the block size to a minimum in order to increase the number of blocks which could be printed on the page. Space is provided to insert seven vertical lines between adjacent blocks, and ten horizontal lines.

The *717* printer, which is the standard line printer for the *704* and *705*, has 120 type wheels, thus the maximum number of characters that can be printed across the page is 120. The length of the page is determined in a sense by the width, since the final aspect ratio must approximate a "B" size drawing (17×22 inches).

Considering the space that must be allowed for off-page line names, for lines between the blocks, and for other necessary identifying information, the optimum page size was chosen as 120 characters by 186 characters. This results in a 5×9 array of circuit blocks.

The vertical size of the page could be increased without limit, of course, merely by printing more lines. The horizontal dimension could be increased by turning the type faces 90 degrees on the type wheels, thus interchanging the width and length. In either case, however, the desirable aspect ratio is destroyed.

The vellum produced on the printer is 15×24 inches. During development and

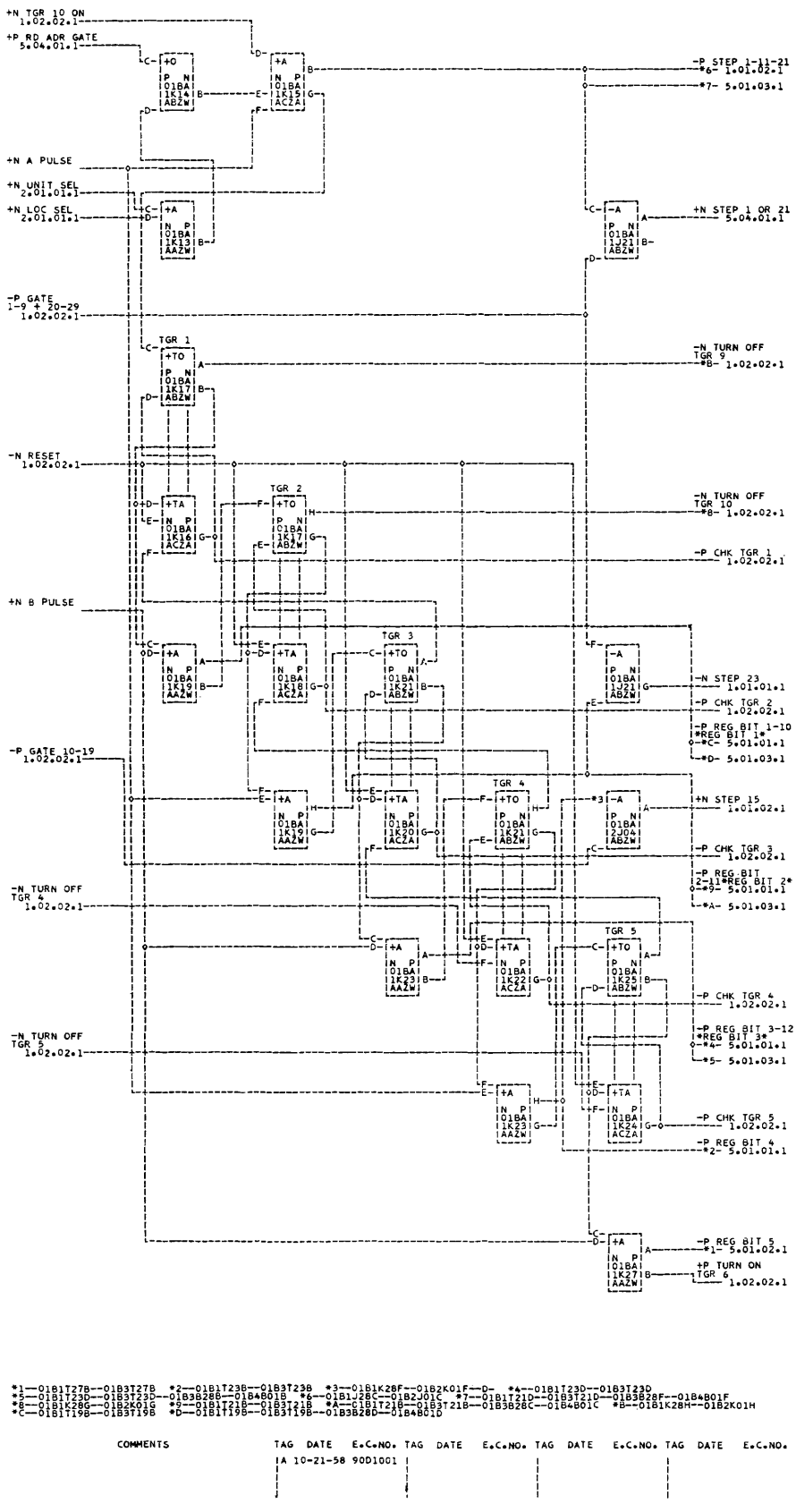

Fig. 5(A). Machine-printed systems page

pilot engineering stages, these drawings are used directly or reproduced in small quantities. For larger volume production and for use in the field these drawings are reduced to 11×17 inches ("B" size).

Spatial Arrangement of Circuit Blocks

The print program does not in any way alter the spatial arrangement of the circuit blocks, producing a page identical (as far as the logic blocks are concerned) to the logic sketch sheet which the engineer designed. The task of arranging the blocks on a page by computer is not insurmountable, but two disadvantages would be experienced. First, when the engineer receives a page of logic blocks from the printer, which is arranged differently than the page he submitted in the first place, he would have difficulty in following the logic flow. Second, when a page is changed by the addition or deletion of a block, it would be likely that the computer would again rearrange the page spatially. Thus it was decided to preserve the spatial arrangement chosen by the engineer.

Spatial Arrangement of Circuit Lines

Although the arrangement of the circuit blocks is not altered by the computer, except on request, the print program does route all the electrical lines on the page. It was found to be cheaper and faster to specify the lines by computer than to record the co-ordinates of all line segments as drawn by the engineer and reproduce the lines when the page is printed. Furthermore, the recording of the lines is a manual job, subject to human error.

Line Representation

Six special characters have replaced standard symbols on the *717* type wheel. These are shown in Fig. 8. The corners enable lines to bend in any direction. The diamond denotes a junction of two lines. Line crossings are represented by a conventional plus symbol. Vertical and horizontal dashes makes up line segments.

Page Image in Memory

An exact image of the final page is developed in memory, character by character. This necessitates a memory allocation of 22,320 characters (120×186) independent of computer aud printed instructions. It takes an average of 45 seconds of computer time to develop a page image in memory and write this image on tape for off-line printing. It takes 75 seconds to print each page on the 150-line per minute off-line printer.

Logic Checking Program

Objectives

The checking program is designed to verify that the logical configuration con-

forms to a set of rules specified by the engineer. Secondarily, of course, the checking program must also detect (and where possible, correct) the errors introduced into the system by the manual processes previously described.

The design rules can be divided into three categories:

1. Circuit rules (Appendix I).
2. Logic format rules (Appendix II).
3. Packaging rules (Appendix III).

Circuit Rules

The circuit rules involved detailed examination of the circuit interconnections to ensure that workable circuit combinations exist. This is called a "circuit compatibility" check. A good deal of effort has been expended in this area to indicate and spotlight the specifics of the incompatibility so that the engineer can identify and correct the difficulty with as little time expenditure as possible. It was felt that a simple yes or no answer to the compatibility question would be too expensive in terms of engineering man-hours.

It should be noted that the philosophy of the program is to identify deviations from the rules and call them to the attention of the designer. When sufficiently sophisticated programs are available, a different philosophy in which the computer does a good deal of the initial design will obviously be in order.

Logic Format Rules

These rules involve checks to ensure that the proper logic format has been followed in minute detail in the finished logic drawings. These rules make possible and useful the machine-produced logic drawing described previously. If this checking were not done, the machine drawing would be only a neat version of the designer's sketch, with the possibility of errors added in preparing it for processing. As a result of this checking, it is assured that the logic is presented in a uniform manner and that it is accurately described. Transpositions of characters and clerical errors are eliminated, making the logic description a reliable document for designing and servicing, and enabling it to serve as an accurate information source for the automatic preparation of necessary secondary documents.

Packaging Rules

These rules take advantage of the SMS concept to ensure consistent, accurate packaging of circuits. Included is a check of the placement of circuit cards in proper relationship to each other and the frame, as well as conventions of wiring interconnections between circuits. A high degree of cabling standardization has eliminated the need for many special cable designs. The checks insure that

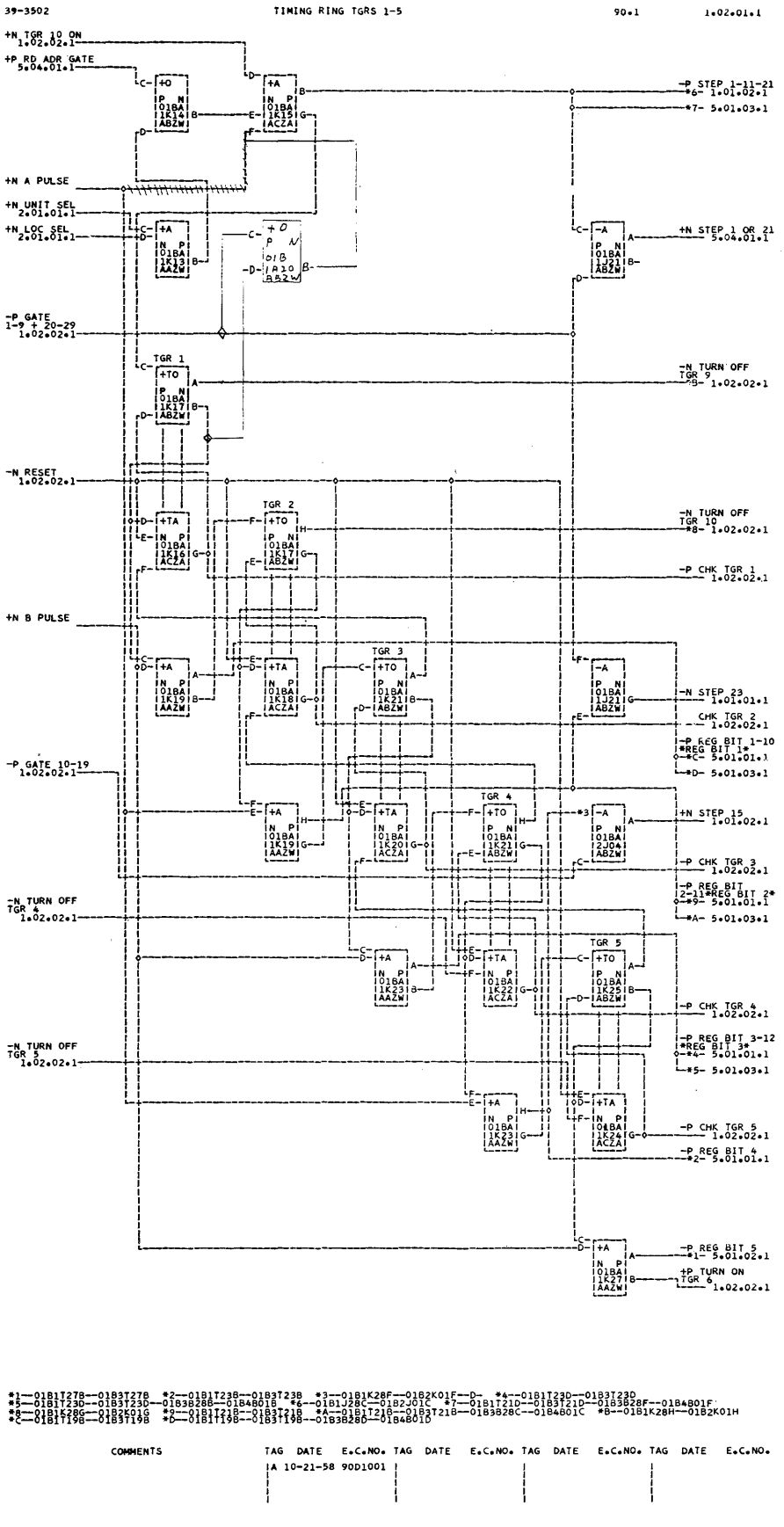

Fig. 5(B). Machine-printed systems page, with manual corrections

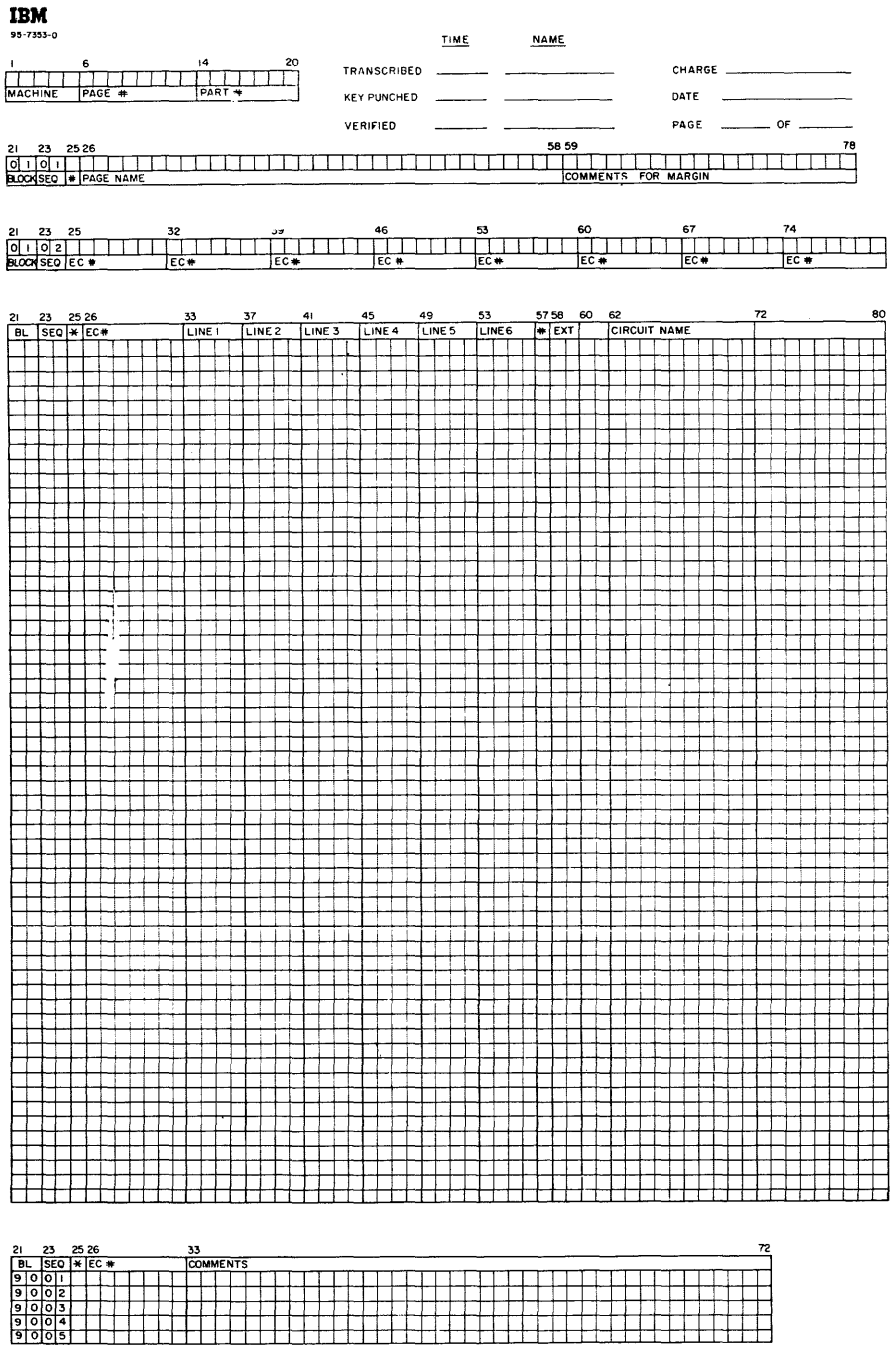

Fig. 6(A). Transcribing form

the designs carefully follow standard rules.

Errata Listing

The primary output of the checking program is the errata listing which is returned with the printed page to the engineer.

Fig. 9 is a compilation of typical errors found by the checking program. It should not be construed to be representative of the numbers of errors made on any given page. The information is organized by logic page, since this is the basic reference document.

Other Output Documents

Another purpose of the checking program is to prepare the many derivative output documents needed to manufacture and service a large computer. The secondary outputs are obtained at this stage in the design mechanization system for two reasons:

1. By its nature the checking program is required to organize the logic data in various formats and sequences.

2. The secondary output documents are useful only if the logic passes the various tests which are imposed by the checking program.

Some of the outputs which are derived from the logic record are as follows:

1. Location charts for the placement of circuit cards.

2. List of points to be connected in wiring panels.

3. Lists of connector jumpers needed to interconnect panels.

4. Lists of cable wires used to interconnect frames and gates.

5. Bills of material for electronic parts.

6. Miscellaneous statistical data.

Operation of Checking Program

The checking program is really a series of individual programs interlocked in a complex manner. The significant components follow.

FORMLO (Format of Logic)

This is a program to reform the master tape records into a format more suitable for the checking process.

CONPAG (Connect Pages)

This program combines lines which are referenced from one page to another. As might be expected, this is a problem area. Three things are done to ease this problem.

1. When matching lines, the names are compressed so that blanks, periods, and commas are eliminated. This prevents mismatches due to the trivial differences in spacing or punctuation.

2. When only one reference is made between two pages, the names are assumed to match. However, a warning message is printed to the effect that this has occurred.

3. When no match can be found, all names are listed together so that the differences are obvious and easily corrected.

LOGVER (Logic Verification)

This program does the circuit checking, such as legality of circuit symbols, accuracy of interconnections, accuracy of representation, etc.

PANLOC (Panel Locations)

This program furnishes a location chart of circuit cards by panel and bills of material for ordering purposes.

PW Edit

This program provides a list of connector points properly arranged for a subsequent program that will determine the actual wire routing to be used.

Sort Programs

These are for the most part standard generalized sort programs written by the IBM Applied Programming Group.

Operating Times

Experience to date shows that for average quantities of input data, the computer time for processing each logic page averages one minute, or from 3 to 4 seconds per circuit block. This is a complete run through the entire complex of programs.

Wiring Program

As discussed previously, the logic sketch sheets are the only input to the design mechanization system. From these diagrams, the checking program prepares on tape, a list of points to be connected, section by section, with back panel wiring. This tape is used as the input to the wiring program which determines the routing of the back panel wires, observing certain restrictions which have been imposed, and produces the wiring list exhibited in Fig. 10. The program also summarizes the panel wires used by length and type, as shown in Fig. 11, to give an effective bill of material for the panel wiring.

Rules for Back Panel Wiring

The high-speed drift transistor circuits used in the *7000* series computers require extreme care in the point to point wiring. Routing arrangements must be found that satisfy the following criteria:

1. Minimize wire length to avoid electrical delays due to capacitance to ground.
2. Minimize the use of shielding to avoid electrical delays and to decrease cost.
3. Maximize isolation of one circuit from another to minimize noise interference.
4. Minimize the number of connectors to a terminal in order to utilize wire wrapping techniques.

The first pass of the program routes wires so as to minimize total wire length. Yellow single-lead wiring is used throughout. A check is then made on interwire noise, and violations of the specified limits are satisfied automatically by rerouting, by using twisted pairs, or, finally, by resorting to coaxial cable.

Since the number of interconnections for the SMS panels varies from 300 to 1,200, and because of the stringent design restrictions, manual routing taxes human capacity. But the wiring program has been averaging about 20 minutes on the *704* for the typical SMS panel.

Engineering Changes

Since design changes in the logic very often require changes in back panel wiring, the system must accommodate changes as introduced by marked up systems pages. Transcribing of engineering changes is minimized, since only alterations to the previous drawing need to be keypunched. The tape updating program makes the necessary alterations to the tape records, and new diagrams are produced by the print program.

Because a slightly changed set of initial conditions might very well result in an entirely different wiring arrangement, and since it would be prohibitively expensive to rewire a complete panel for each design change, the wiring program must superimpose the required changes on an existing arrangement, without violating any of the rules. Here again the computer reduces to trivia a problem which is excessively complex by manual methods. Changing circuit designs are, generally, readily incorporated into the programs. Consequently, with experience and advances in circuit technology, conformance with the new standards can be checked readily.

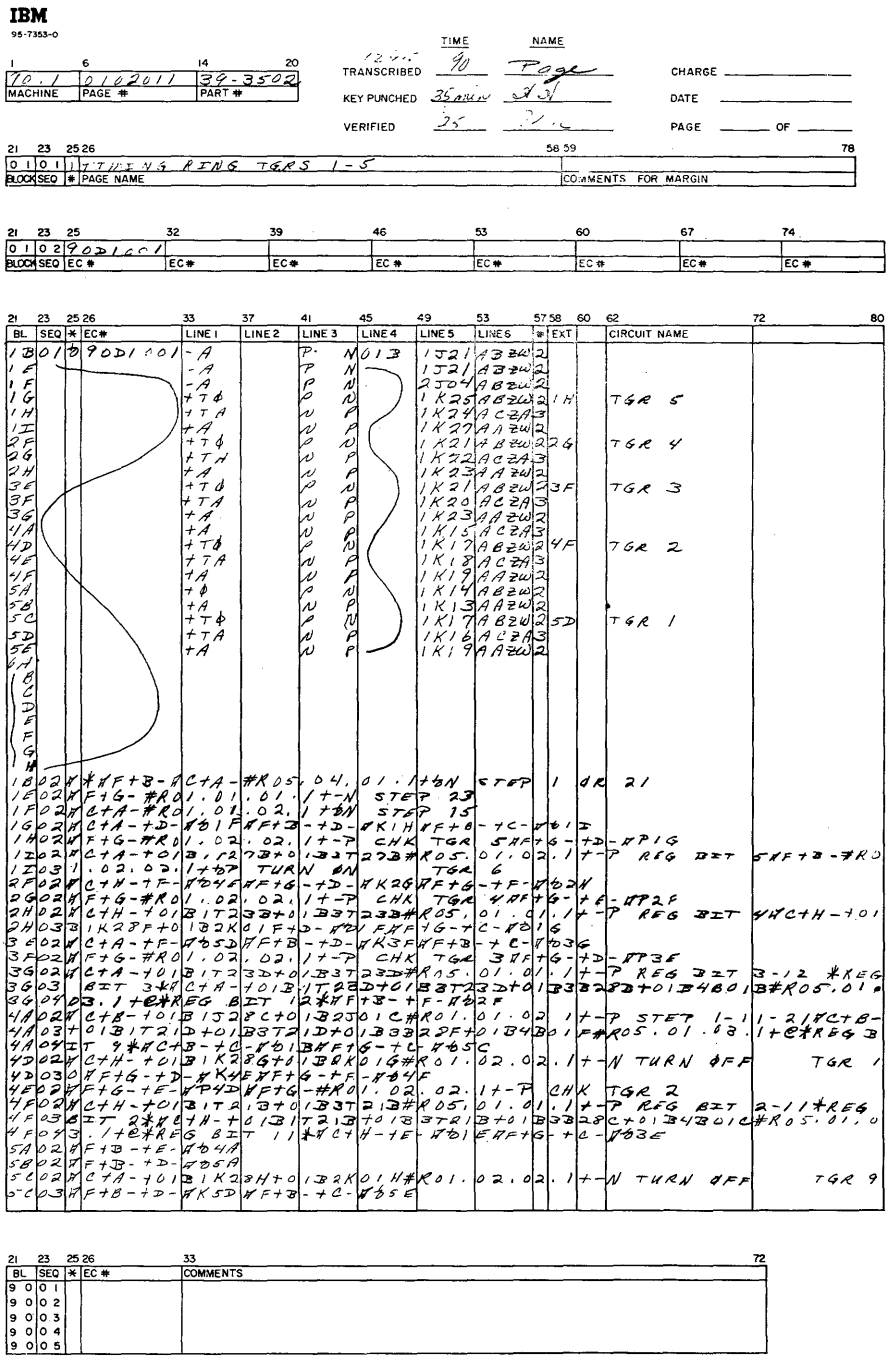

Fig. 6(B). Sample entries on transcribing form

Summary

Advantages

The design mechanization system offers the following advantages:

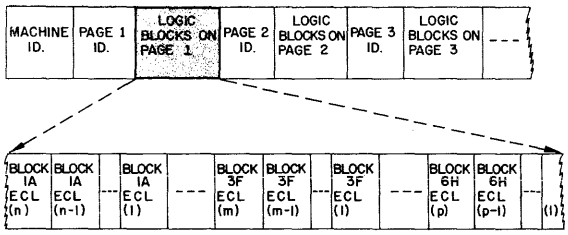

Fig. 7 (left). Master tape format

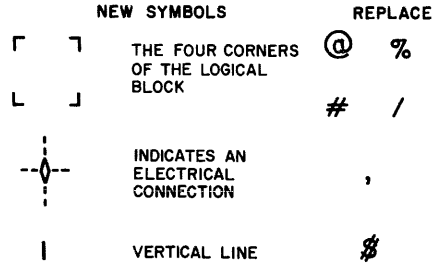

Fig. 8 (right). Special symbols for the printer type wheel

1. Elimination of error
2. Less repetitive manual detail work
3. Speed of processing
4. More comprehensive information

Elimination of Error

Because of the immense amount of detailed information which must be gathered, preserved, and disseminated during the life of a development project, human errors are inevitable. Many of these errors are not detected in the making, and result ultimately in malfunctions of the machine, scrap and rework, and high product engineering and engineering change activity. The mechanized system not only replaces fallible manual procedures with accurate automatic procedures, but also isolates and rejects many of the errors made in the remaining manual processes.

Less Repetitive Manual Detail Work

Much of the routine work of abstracting details from the basic design is eliminated, leaving professional engineers free for more creative work. This amounts to a more effective utilization of engineering manpower.

Speed of Processing

Waiting periods are eliminated in many stages of the project. Logic diagrams designed by the engineer are checked, "drawn," and returned without delay. Wiring lists are prepared immediately after the design is completed. Bills of material and statistical information are compiled on demand. Changes to circuits and wiring are incorporated without delay. In an era where time is money and overhead is excessive, the elimination of costly delays can reduce over-all project budgets substantially.

More Comprehensive Information

The recording of all logic data on the master tape provides an opportunity to obtain design information heretofore difficult to compile. Most significant to date has been the statistical data so necessary for cost engineering and standardization. A complete count of transistors, circuit cards classified as to type, and various other components can be obtained in a matter of minutes. Moreover, by studying on a statistical basis the utilization of the standard circuits, it becomes possible to eliminate rarely used components and redesign others for more general utility. A reduction in the standard circuit manual is a very desirable objective.

An additional advantage is the availability of logic diagrams at various engineering change levels, thus eliminating a costly storage operation.

Disadvantages

The system as it now exists is not without disadvantages. Some of these are:

1. Programming cost is high, and several man-months of programming effort can be obsoleted by changes in design. This can be a risk when working in a development area where change is the rule rather than the exception.
2. The circuit block representation, a somewhat inflexible 5×9 format, is not optimum for representing all the necessary logic. This can sometimes increase the number of logic documents needed.
3. The transcribing and keypunching operation has proven to be extremely time consuming. A large volume of data must flow through this input system with complete accuracy.

Operating Times

These vary with the volume and complexity of the logic records. Based on experience to date, average figures are as follows:

$2\frac{1}{2}$ to 3 man-hours to transcribe and keypunch a logic page entry. 1 minute of computer time to add to or alter the master tape record. 45 seconds of computer time to prepare the print image on tape. (An additional minute of off-line operation is required for the actual printing.) 70 seconds per logic page checked by the checking program. 20 minutes for computing the wiring of a typical panel.

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                    AUTOMATION OF DESIGN - POUGHKEEPSIE
                      DEVIATION FROM DESIGN STANDARDS
MACHINE # -50-1                OCTOBER 20, 1958                    2.25.08.1 A

THE FOLLOWING LINES HAVE NOT BEEN CONNECTED BECAUSE NAMES CANNOT BE MATCHED
                LINE NAME                          FROM PAGE
     N NOT C1-NOT  C2 NOT C4                       2.25.03.1

BLOCK 3A COMBINATION DQ-- CANNOT DRIVE BLOCK 2A COMBINATION DNYG ON THIS PAGE
      3C             DQ--                         2C             DNYG ON THIS PAGE

THE FOLLOWING LINES ARE NOT LOADED
     FROM BOX LOC ON BLOCK
              D        3A

AN IMPROPER COMBINATION OF PINS HAS BEEN DESIGNATED FOR THESE BLOCKS
                                  4G

STUB INCORRECTLY DESIGNATED ON BLOCK  3A
                                      3E

CONNECTOR MISSING ON THE FOLLOWING LINES
         FROM PIN BLOCK
                   2C       3E TO PAGE 2.36.06.1

THE FOLLOWING CIRCUITS HAVE TOO MANY COUPLING NETWORKS
                                  BLOCK   CKT   CARD CAP
                                    2C     DP     DNYG

THE FOLLOWING LINES ENTERED THIS PAGE MORE THAN ONCE--CONNECTION HAS BEEN MADE
                LINE                   FROM PAGE
     P 16SR1 TURN  ON SR2 32 TGR       3.20.02.1

THE FOLLOWING BLOCKS DRIVE THEMSELVES
                                  2I

THE FOLLOWING BLOCKS HAVENT BEEN PROCESSED BECAUSE OF AN ERROR IN RECORD FORMAT
                                  3C

THE FOLLOWING LINES HAVE NOT BEEN CONNECTED
                LINE                              PAGE
     P TURN ON EMAR 32 TGR PCW SR1     FROM     3.30.04.1

THE FOLLOWING LINES ARE OVERLOADED
     FROM BOX LOC ON BLOCK
              C        2F

AN IMPROPER PIN DESIGNATION HAS BEEN MADE
                        PIN       BLOCK
              OUTPUT     B         3I

THE CIRCUIT NAME APPEARING ON THE TOP LINE IN THESE BLOCKS IS NOT STANDARD
                                  3E

CONNECTORS NOT PROPERLY DESCRIBED
       CONNECTOR ON LINE FROM PIN ON BLOCK
        03D2D28D                   B       3B

THE FOLLOWING BLOCKS WERE NOT TRANSCRIBED
                                  1B

AN IMPROPER TRANSISTOR TYPE HAS BEEN SPECIFIED ON THE THIRD LINE IN THESE BLOCKS
                                  3A
```

Fig. 9. Machine-printed errata listing

INTERNATIONAL BUSINESS MACHINES

AUTOMATED WIRING LIST NO. 2539-88 MACHINE 7000.20.1 PG 7 11-03-58

ENG. CHG. 03

FR	G	P	NET	LGTH	FROM	VIA	VIA	TO	FR	TO	TYPE
01	B	1	36	1 3/8	J16A			J18A			Y
01	B	1	33	2 5/8	J16C		J20C	J21D			Y
01	B	1	38	0 7/8	J16D			J17B			Y
01	B	1	15	2 7/8	J16E			J21E			Y
01	B	1	20	0 7/8	J16F			J17H			Y
01	B	1	18	2 3/8	J16H		K16□	K16A			Y
01	B	1	38	0 5/8	J17A			J17B			Y
01	B	1	37	1 1/8	J17D		J17F	J18H			Y
01	B	1	19	3 7/8	J17E		K17E	K16H			Y
01	B	1	20	0 5/8	J17G			J17H			Y
01	B	1	34	1 1/8	J21B	J21A		J22A			Y
01	B	1	16	2 3/8	J21G			K21A			Y
01	B	1	2	0 5/8	K05A			K05B			Y
01	B	1	2	0 7/8	K05A			K06C			Y
01	B	1	3	0 7/8	K06B			K07D			Y
01	B	1	5	1 3/8	K06D	K07B		K08B			Y
01	B	1	3	1 1/8	K07D	K07C		K08C			Y
01	B	1	6	1 3/8	K08A			K10A			Y
01	B	1	3	2 7/8	K08C			K13C			Y
01	B	1	8	0 7/8	K08D			K09B			Y
01	B	1	8	0 5/8	K09A			K09B			Y
01	B	1	7	1 1/8	K09D		K09F	K10H			Y
01	B	1	10	0 5/8	K09G			K09H			Y
01	B	1	10	2 1/8	K09G	K11D		K13D			Y
01	B	1	11	1 1/8	K13B	K13A		K14A			Y
01	B	1	39	4 7/8	H02K		J02□	J06H	H02J	J06J	T

Fig. 10. Machine-printed back panel wiring list

INTERNATIONAL BUSINESS MACHINES

AUTOMATED WIRING LIST NO. 2539-88 MACHINE 7000.20.1 PG 10 11-03-58

ENG. CHG. 03

BILL OF MATERIAL

NUMBER OF WIRES EACH	LENGTH IN INCHES	TYPE OF WIRE
001	7 5/8	C
002	7 7/8	C
001	8 1/2	C
001	8 1/4	C
001	8 1/8	C
001	9 3/8	C
001	10 1/8	C
001	10 7/8	C
001	11 1/2	C
002	11 3/8	C
001	11 5/8	C
001	11 7/8	C
002	12 3/4	C
002	12 3/8	C
002	12 5/8	C
001	13 1/4	C
001	13 1/8	C
001	13 3/8	C
001	13 5/8	C
001	15 7/8	C
001	18 1/2	C
001	4 7/8	T
048	0 5/8	Y
029	0 7/8	Y
025	1 1/8	Y
011	1 3/8	Y
003	1 5/8	Y
002	1 7/8	Y
001	2 1/8	Y
004	2 3/8	Y
003	2 5/8	Y
010	2 7/8	Y
003	3 1/2	Y
007	3 1/8	Y
001	3 3/4	Y
007	3 3/8	Y
012	3 5/8	Y
003	3 7/8	Y
005	4 1/8	Y
001	4 7/8	Y
001	5 3/8	Y
001	5 5/8	Y
001	5 7/8	Y
001	6 1/8	Y

Fig. 11. Machine-printed summary of panel wiring for bill of material use

Extensions of Design Mechanization

For the first time, a complete logic record of a large computer exists in readily available digital form. Problems arising in the post-release period can be programmed readily to make valuable use of this information; for example, to help design special features and to derive proper data for controlling automatic production machinery.

It is obvious that much more progress remains to be made in this direction. By and large IBM has succeeded in mechanizing a record-keeping system. The engineers' effort has been channeled into concern primarily with the basic source document, the logic sketch sheet. Logical extensions of the present program are obvious.

It was not many years ago that "computer-designed computers" seemed like an idle dream. The authors feel that the completion of the record-keeping system described here is a significant step toward this goal.

Appendix I. Checking Program, Circuit Rules

The following lines leaving this page have been defined more than once:

Two or more lines leave a page from different logic blocks but have the same name.

An improper pin designation has been made:

For the specified card/cap combination, the pin given is incorrect.

The circuit name appearing on the top line in these blocks is not standard:

The circuit name given has not been approved. (Also: the name given may be positioned incorrectly within the block.)

An improper transistor type has been specified on the third line in these blocks:

For the specified card/cap combination, the transistor type indicated is in error.

Block xx combination xxxx cannot drive block zz combination zzzz.

Illegal connection between circuits. Existing rules do not permit the indicated circuit to drive the other.

The following lines are overloaded:

Circuit drives more than it should.

The following lines are not loaded:

Coupling network not present.

Nonstandard card/cap combination for driving block no further checking has been done on these blocks:

The card/cap does not appear in the tables used by the checking program.

The following lines to a block with nonstandard card/cap have not been checked:

Since the card/cap of the driven block is not standard, lines connecting other blocks cannot be checked.

The following pins are not at the proper location on the circuit block:

When a particular pin must appear at a definite location on a logic block, a violation is indicated in this manner.

Driver output line type disagrees with driven input:

Level on output line of driving circuit disagrees with level on input line of driven circuit.

Stubs not allowed on block:

Stub placed on logic block which does not allow a stub.

The following circuits have too many coupling networks:

Two or more coupling networks have been indicated.

Appendix II. Checking Program, Logic Format Rules

These blocks have not been processed because of an error in record format:

These include errors found in the records

taken from the master tape by the print-preparation program (e.g. pages which are not numeric, incomplete information, incorrect block designation, etc.)

The following lines have not been connected because names cannot be matched:

More than two lines between pages, some of which may have been connected. The lines indicated are those where it has not been possible to determine whether connection could be made.

The following lines cannot be connected:

Lines that indicate a particular page as a destination, but on the designated page no reference has been made for a line coming to it from the other page.

These lines have no page designation:

Lines that enter or leave a page without specifying the page from which the line is coming or to which it is going.

Names for the following lines are missing:

Lines have not been identified by names where it is necessary to do so.

The following lines leaving this page have been connected, however the line names are unequal:

Occurs when there is only one line reference between two indicated pages even though there are differences in line names (i.e. blank spacing, use of period in abbreviation, additional comments); the program considers it appropriate to connect the indicated lines.

The following lines entered a page more than once:

Lines with the same name and page source have entered a page at two separate places on a page when the line should have entered at one location and branched after entering.

A line from the following blocks leaves the page on the left contrary to drawing standards:

Output lines from logic blocks shown leaving a logic page should be drawn going off the right side of the page.

Stub incorrectly designated on block:

A stub is permitted on the logic block, but it has been shown in the wrong location.

The record character count for the following blocks is incorrect:

The number of characters in a master tape record does not agree with the number of characters received to be checked.

The following block drives itself:

The indicated block is its own input (probably transcription error.)

These blocks have not been transcribed:

One or more lines on a page refer to a block which does not exist. (The block may not have been transcribed, or it may have been deleted but information about a line which drives it was not deleted.)

Appendix III. Checking Program, Packaging Rules

Machine location incomplete for the following blocks:

One or more items of the information identifying frame, gate, panel, row, or column is not present.

The machine location of the following blocks is incorrect:

One or more parts of the indicated machine location have been specified incorrectly.

An improper combination of circuit pins has been designated for these blocks:

One or more of the pins designated for a particular logic block have been indicated incorrectly.

The following blocks have identical machine locations:

Two or more logic blocks have been given the same machine location assignments.

Connector missing on the following lines:

Connectors should be indicated since the line connects blocks in different panels.

Connectors on the following lines have not been checked:

Because of other errors or incomplete information some lines cannot be checked for necessary connectors.

Connectors not properly described:

The information given does not describe any type of connector.

Ground pin used for connector:

Any connector which uses a ground pin is indicated.

The row, column, or pin of the following connectors do not match:

Where it is necessary for the row, column, or pin of a pair of connectors to agree, this has not been indicated.

Edge connectors join the same or adjacent gates:

A connector should be used, but not an edge connector.

Discussion

Frank Segal (Westinghouse Electric Company): Is IBM planning to distribute this through Share?

Mr. Case: This is a series of programs of a high degree of complexity. I doubt if we are going to distribute it through Share, but we are certainly willing to donate it to anybody who feels that they can use it. We have nothing to hide and everything to gain by encouraging the use of computers.

Peter Scola (General Electric Company): What techniques are you using to minimize wire length?

Mr. Case: Wire length is minimized by selecting from a list of possible paths, the paths which will result in a minimum total length. Two points to be connected lie on opposite vertices of a parallelogram, and all paths on the edges or paths within the boundaries with two bend points have equal lengths. This enables a decision to be made selecting the least noisy path without increasing the length above the minimum.

Question (Bell Telephone Laboratories): Briefly, what is your tape update program? Do you have to run off another set of cards to attain a block omitted previously?

Mr. Case: The question refers to program organization. This is a standard file maintenance operation, using the old tape file as input, and adding or deleting any blocks from card input to produce a new output tape.