IBM

Customer Engineering Reference Manual

Tape Adapter Unit

IBM Customer Engineering Reference Manual

Tape Adapter Unit

MAJOR REVISION (January, 1961)

This edition, Form 223-6867-2, obsoletes Form 223-6867-1 and earlier editions. Significant changes have been made throughout the manual, and this new edition should be reviewed in its entirety.

IBM Tape Adapter Unit

Contents

Section 1. SCHEDULED MAINTENANCE
This section discusses scheduled maintenance objectives and visual inspection procedures 5

Section 2. DIAGNOSIS
This section contains troubleshooting methods and diagrams to be used to locate faulty components within the unit. Checking circuits and diagnostic control functions are also included 7

Section 3. CONDENSED LOGIC
This section contains logic and data flow diagrams for the major operations of the unit and also timing sequence charts 9

Section 4. SERVICING PROCEDURES
This section includes typical waveforms and marginal checking procedures 33

Section 5. SERVICE AIDS
Machine locations are given in this section, together with packaging differences between TAU I and TAU II. Special circuit information, including final amplifier and clipping level checking, is also given 35

Safety

Personal safety cannot be overemphasized. To insure your safety, make it an everyday practice to follow all safety precautions at all times. Become familiar with and use the safety practices outlined in IBM Form 124-0002, a pocket size card issued to all customer engineers.

For specific safety precautions concerning TAU and its associated circuitry, consult the service manuals for the machine in which TAU is packaged.

1.1 Scheduled Operations

The Tape Adapter Unit (TAU) is not a complete machine unit; scheduled maintenance required by its circuitry is incorporated into the operations set up for the machine unit in which TAU is packaged. For such operations, see Section 1 of the manual for the machine unit.

1.2 Cleaning

Do not clean or disassemble TAU during any scheduled maintenance operation unless absolutely necessary. Unnecessary cleaning often results in more harm than good because of the possibility of breaking solid wires, bending card receptacle pins and installing printed circuit cards in the wrong socket. If air filters are changed as required in the packaged unit containing TAU circuitry, cleaning will not be required.

1.3 Visual Inspection

Visual inspection is an important part of every maintenance operation. Whenever TAU circuitry is looked at, see that:

1. All printed wiring cards are seated firmly in their sockets.
2. There are no loose wire ends, metallic chips, or improper wire wrapping which might cause short circuits.
3. There are no frayed, damaged, or broken wires or cables.
4. All cables and coaxial lines are supported, laced, and have enough slack for servicing.
5. There are no bent socket pins on the reverse side of each card receptacle.

1.3.1 Inspecting Printed Wiring Cards

Cards should be removed from their receptacles only to replace faulty cards or for troubleshooting. When card removal is necessary, inspect each card for:

1. Damaged or burned components (identified by changes in physical appearance, discolored marker bands, or melted wax).
2. Improperly soldered components.
3. Short circuits caused by solder splashes across the printed wiring land pattern.
4. Damaged card receptacles and card guides.
5. Worn, dirty, or damaged connector prongs.

NOTE: Card connectors can be cleaned by rubbing the dirty area with a soft cloth dampened with a cleaning solution, IBM P/N 450608 (trichloroethylene).

2 Diagnosis

Contents

2.1 Approach to Troubleshooting 7
2.2 Diagnostic Programs 7
2.3 TAU Circuits 7
2.3.1 Checking Circuits 7
2.3.2 TAU Clocks 7
2.3.3 Diagnostic Controls 8

2.1 Approach to Troubleshooting

Troubleshooting aids in this manual do not completely cover any one machine but are applicable to a number of machines in which the standard TAU circuitry is packaged.

TAU includes the basic circuits for tape control, but it is not a complete tape control unit; it is not supplied with input-output cables, mounting frame, covers, power supply, or customer engineering test panel. To satisfy system requirements, special features and auxiliary equipment are added to TAU circuitry to complete the over-all machine unit. The troubleshooting aids presented in this section are restricted to TAU circuits only. For the tie-in between TAU and its associated circuitry in any system, consult the reference manual for the machine in which TAU is packaged. That manual will contain specific information applicable to TAU circuits, such as diagnostic routines, indicating lamps, neons, and other means for controlling and moving information through TAU.

This manual describes TAU as existing in the left card chassis frame of a horizontal sliding gate assembly, disconnected from any associated circuitry. It assumes that input signals to the TAU package are within specifications. For machine units in which TAU is in the right chassis frame of a horizontal sliding gate assembly, or in the vertical swinging gate, the physical locations in this manual will not apply. Variations in packaging, however, do not destroy the usefulness of diagrams in describing TAU control, timing, and logic flow.

2.2 Diagnostic Programs

Diagnostic programs for standard TAU circuitry are incorporated in programs written for the machine unit and system in which TAU is packaged. For specific information consult the reference manual for the machine in which TAU is packaged.

2.3 TAU Circuits

2.3.1 Checking Circuits

Check the following circuits periodically and after wiring changes.

A VRC Read-Write TAU Check Trigger: Check the validity of these circuits by using the odd-even redundancy switch and the seven bit switches. All combinations can be explored and the failing circuit detected.

Compare Check: Remove the high clip FC-- final amplifier cards one track at a time. This creates a condition similar to that encountered during a normal write check.

Skew Check: This circuit functions as a check on the write operation. Remove the write driver, one track at a time, from the tape unit. This prevents erasure of previous information resulting in asynchronous flow of read pulses, many of which will cause skew checks.

LRCR: The LRCR character is generated by *write trigger release*. Remove the line driver in TAU to prevent resetting the write triggers in the tape unit, which will cause an LRCR check.

Echo Check: Write a record with the seven bit switches off. This causes write clock cycles without switching the tape unit write triggers, resulting in an echo check.

2.3.2 TAU Clocks

All TAU clocks (read clock, write clock, and delay counter) operate as binary counters.

Read Clock: Check for binary action of the clock by synchronizing on the fall of trigger RC8, and displaying all triggers with the first bit line tied on.

Write Clock: Use the same procedure as for the read clock, except that a continuous write operation will cause the correct action.

Delay Counter: This circuit is the key to motion and record control in TAU and should be checked carefully if trouble is suspected. Check the main action of this circuit by tying up the microsecond or millisecond control lines and synchronizing on the fall of the highest trigger while observing each lower trigger.

The duration of all clocks will depend on the tape unit selected and ready or, if no tape unit is selected, will revert to 729 II low-density timing.

The drive and reset of the delay counter will require tape unit operation. Other operations listed are: write delay, read delay, write disconnect delay, and the sequence of backspace timings. These timings should be checked against specifications by writing, reading, and backspacing single-character records (tape marks).

2.3.3 *Diagnostic Controls*

+N Early Sample (gated on error trigger): Advances turn-on of skew gate trigger by one read clock count in read and write operations. This control is designed to detect marginal skew conditions.

+P Amplifier Bias: In read only, measure read register clipping level at AFC, pin A, −1.30v DC. Reading while writing, measure read register clipping level at AFC, pin A, −1.45v DC. This control is used to detect excessive noise while writing (write feed-through) and low output amplifiers while reading (channel A VRC).

+P Compare Check: When this is gated to the error trigger, for read operation only it compares register A with register B. This control is used to detect excessive noise while reading (cross-talk, base-line shift, high output amplifiers).

+P A Register Only: For read only, this forces register A gate to the read-write register. This is used for the same purpose as +P compare check.

+P B Register Only: For read only, this forces register B gate to the read-write register.

−P Manual Stop on Error: This causes a busy signal, thus preventing the next operation. This is used with the above diagnostic controls to analyze error conditions.

3 Condensed Logic

Contents

3.1	Over-all Logic Flow	9
3.2	TAU Operations	9
3.2.1	Read	9
3.2.2	Read while Writing	9
3.2.3	Write	9
3.2.4	Disconnect	9
3.2.5	Backspace	15
3.2.6	Rewind	15
3.3	Timing, Control and Data Flow	15
3.3.1	Timing Sequence Charts	15
3.3.2	Tape Unit Control Lines	15
3.3.3	Read and Write Data Flow	15
3.3.4	Delay Counter and Clocks	15
3.4	Power Supply Requirements	15
3.5	TAU Oscillators	15

3.1 Over-all Logic Flow

Over-all logic flow within the standard TAU package is shown in Figure 3-1. Each function indicated in this diagram is described in more detail in subsequent sections and diagrams.

3.2 TAU Operations

3.2.1 Read

In this operation (Figure 3-2) TAU receives a read call and develops a tape unit go signal that starts tape motion. A read delay, also initiated by read call, allows the tape unit to reach normal operating speed before reading data. After read delay, the TAU final amplifiers are conditioned to accept information.

Each character read from tape is level sensed and sent to read registers A and B. The first character to enter the read registers turns the read clock on for one complete cycle, and this clock furnishes timing and gating signals to control data flow through TAU during a read operation.

Data input to the read-write register is normally taken from read register A. If an error is detected in this register, however, the read clock conditions the read-write register to stop accepting information from read register A and to read register B. A character set into the read-write register is available as an output.

After each character is read, the read clock (unless it is turned on by the next succeeding character) will start the end-of-operation action. This action includes processing the check character, resetting the read circuits, and stopping tape motion.

3.2.2 Read while Writing (Figures 3-3A and 3-3B)

In this action, the write control circuits initiate a read operation while writing to check for writing errors. Reading while writing enables the operator to detect immediately write operation malfunctions, tape imperfections, and excessive noise. This operation is essentially the same as a normal read operation except that data are not set into the read-write register, and all information checking is done at the read register.

3.2.3 Write

TAU receives a write call and develops a signal that starts tape motion (Figure 3-4). A write delay allows the tape unit to reach normal operating speed before writing data. The write clock is started by write call and conditions the read-write register to be on after write delay.

Write input data lines set the read-write register, and information becomes available to the tape unit. The write clock also generates a write pulse that is sent to the tape unit; this pulse is necessary to initiate writing.

TAU continues writing until interrupted by a disconnect call that completes the write operation, writes a check character, and stops tape motion.

3.2.4 Disconnect

Disconnect call is a signal generated by the system to end the write operation (Figure 3-4). This signal turns on the TAU disconnect trigger which, with the write clock (WC) 14, turns the write delay disconnect (WDD) trigger on and starts the delay counter stepping at the microsecond rate.

When the delay counter counts to WDD 60, the write trigger release and the tape unit write triggers are reset. All write triggers on at this time write a bit as they are reset, thus writing a check character.

Reset of the write trigger release when the WDD trigger is on causes the delay counter to step at the millisecond rate. When the delay counter has counted to WDD 20, both the GO and WDD triggers are reset and the tape unit coasts to a stop. The write trigger remains on until the read check operation is completed to keep TAU in the busy status.

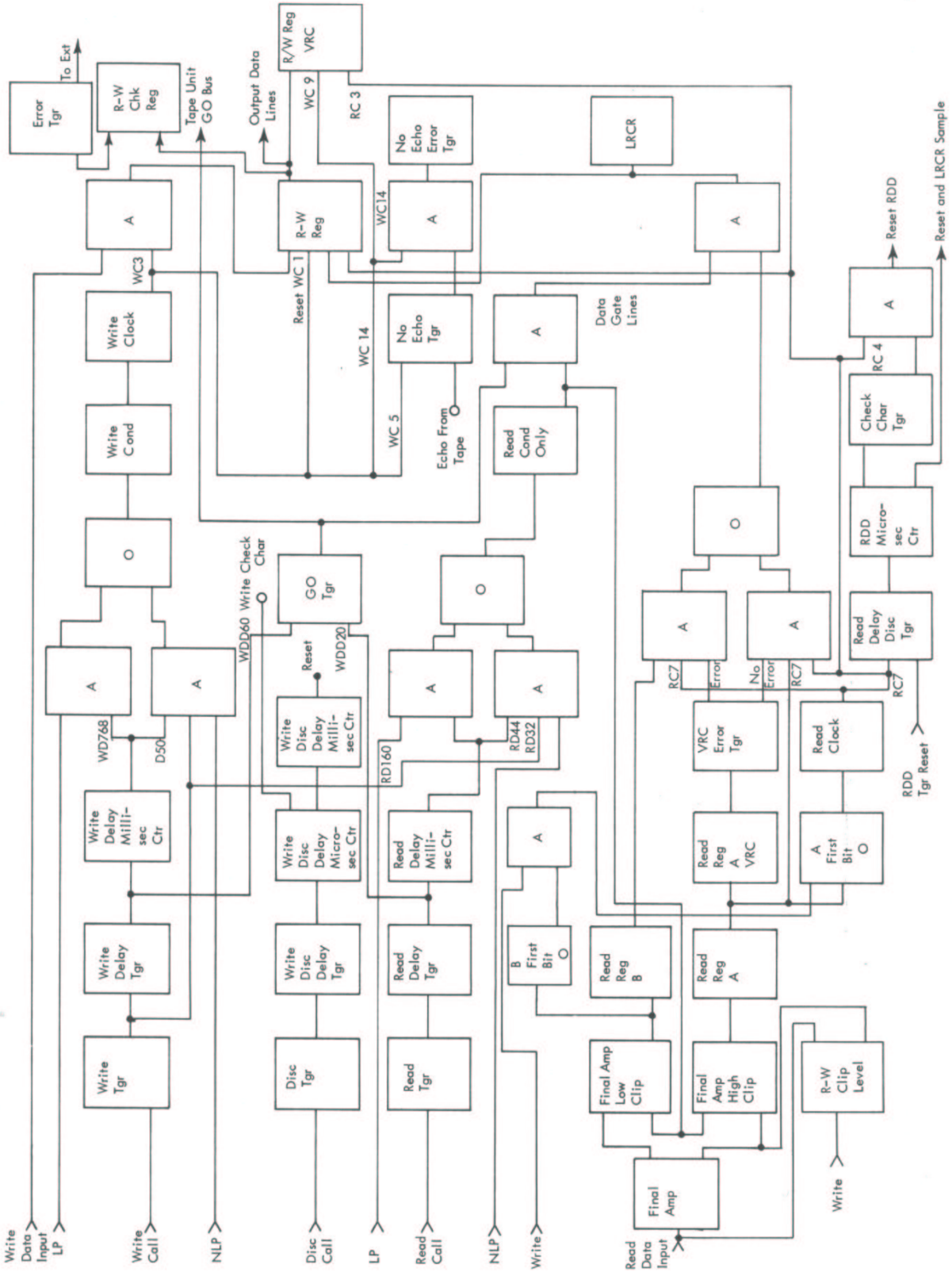


Figure 3-1. Over-all Logic Flow

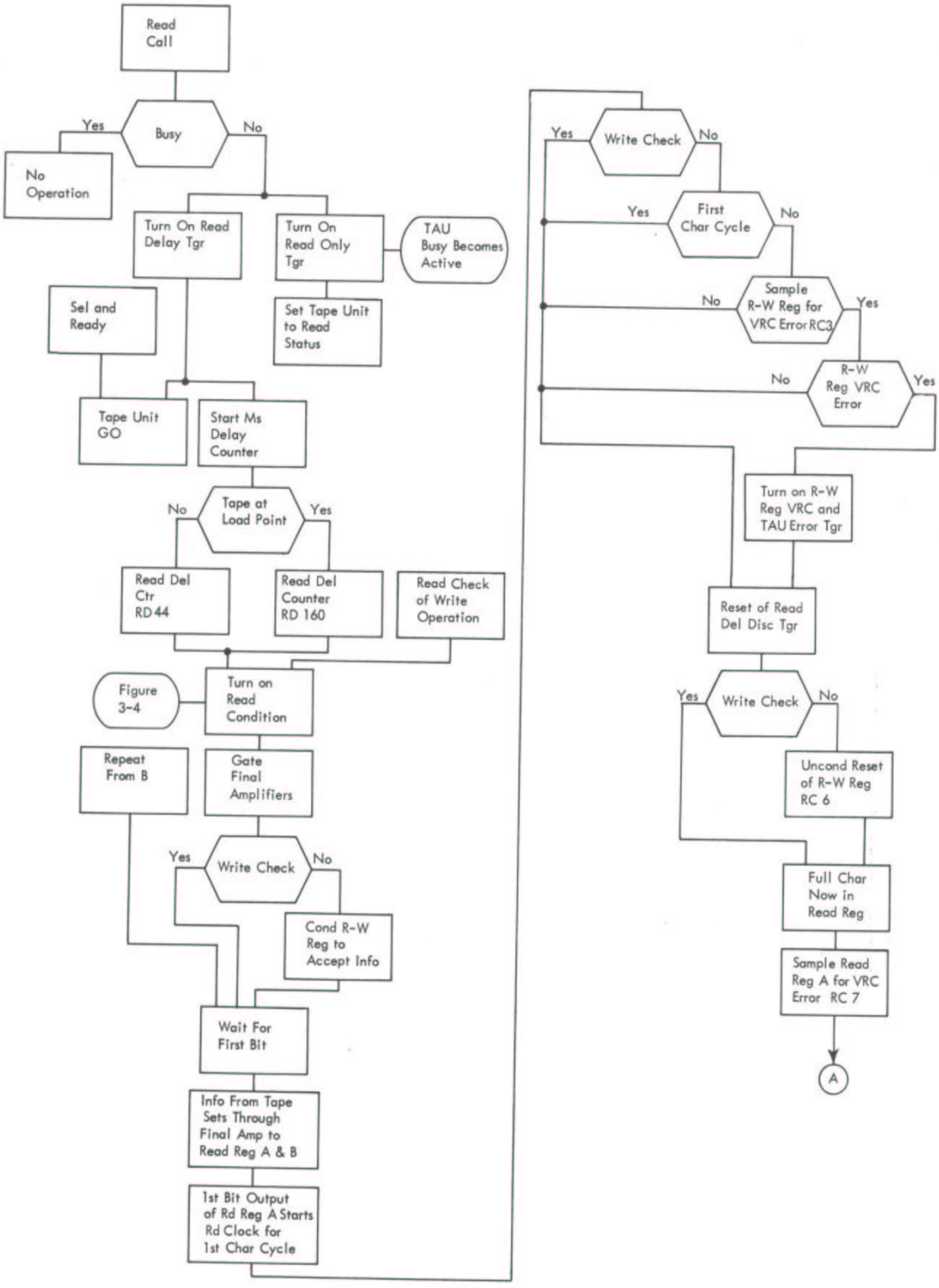


Figure 3-2. Read Call and Write Check Operation

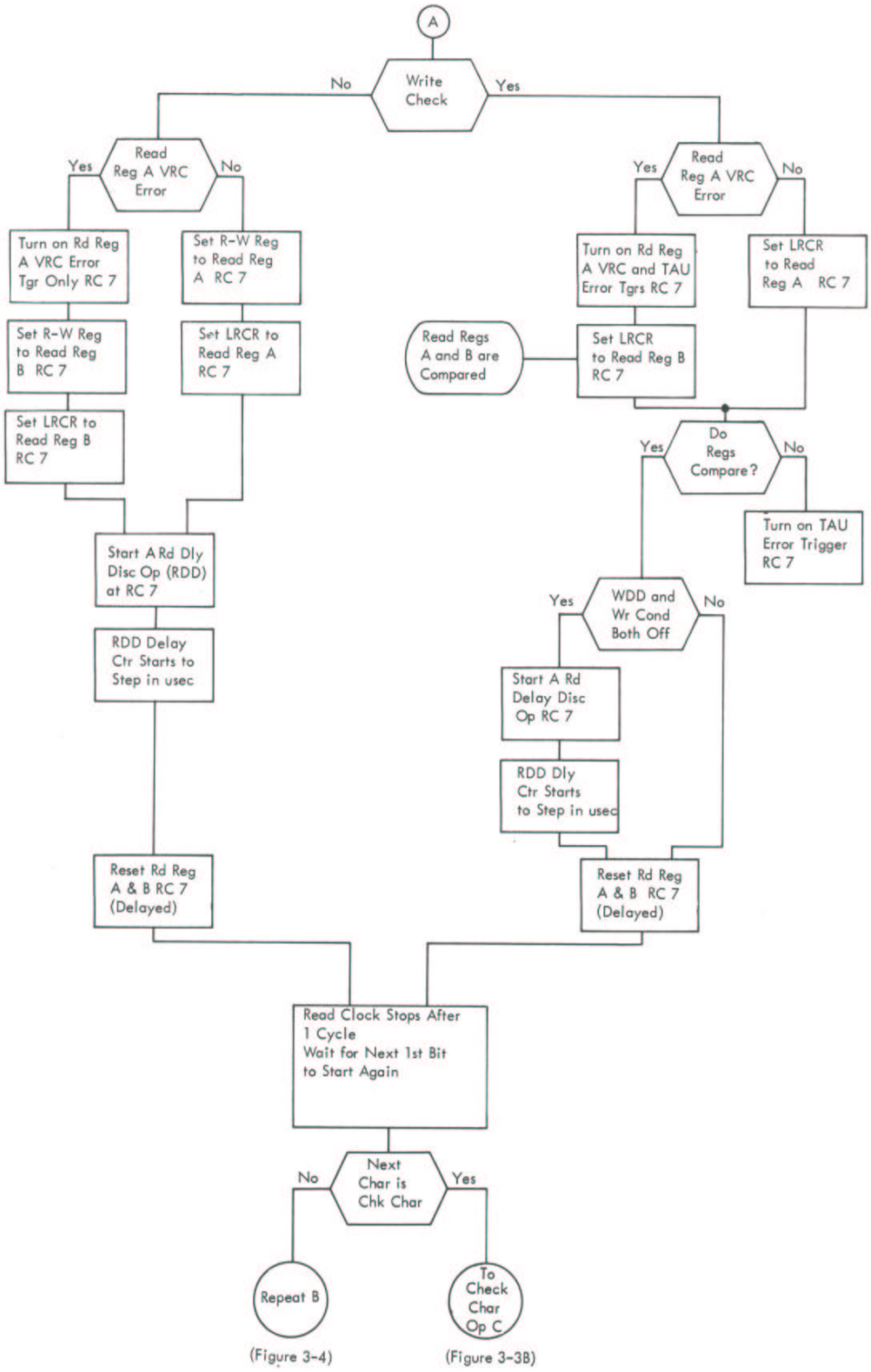


Figure 3-3A. Read and Write Check Operation

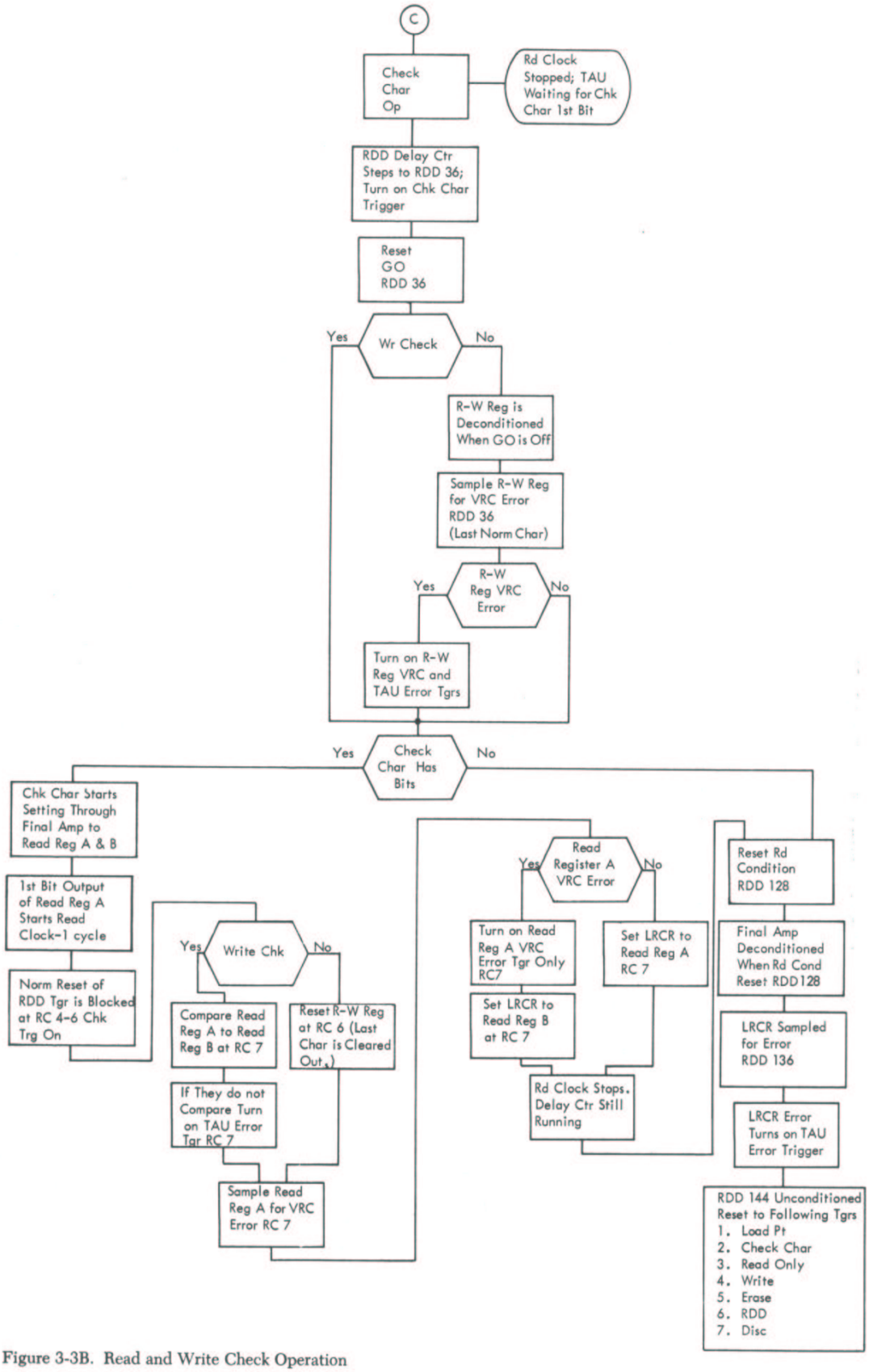


Figure 3-3B. Read and Write Check Operation

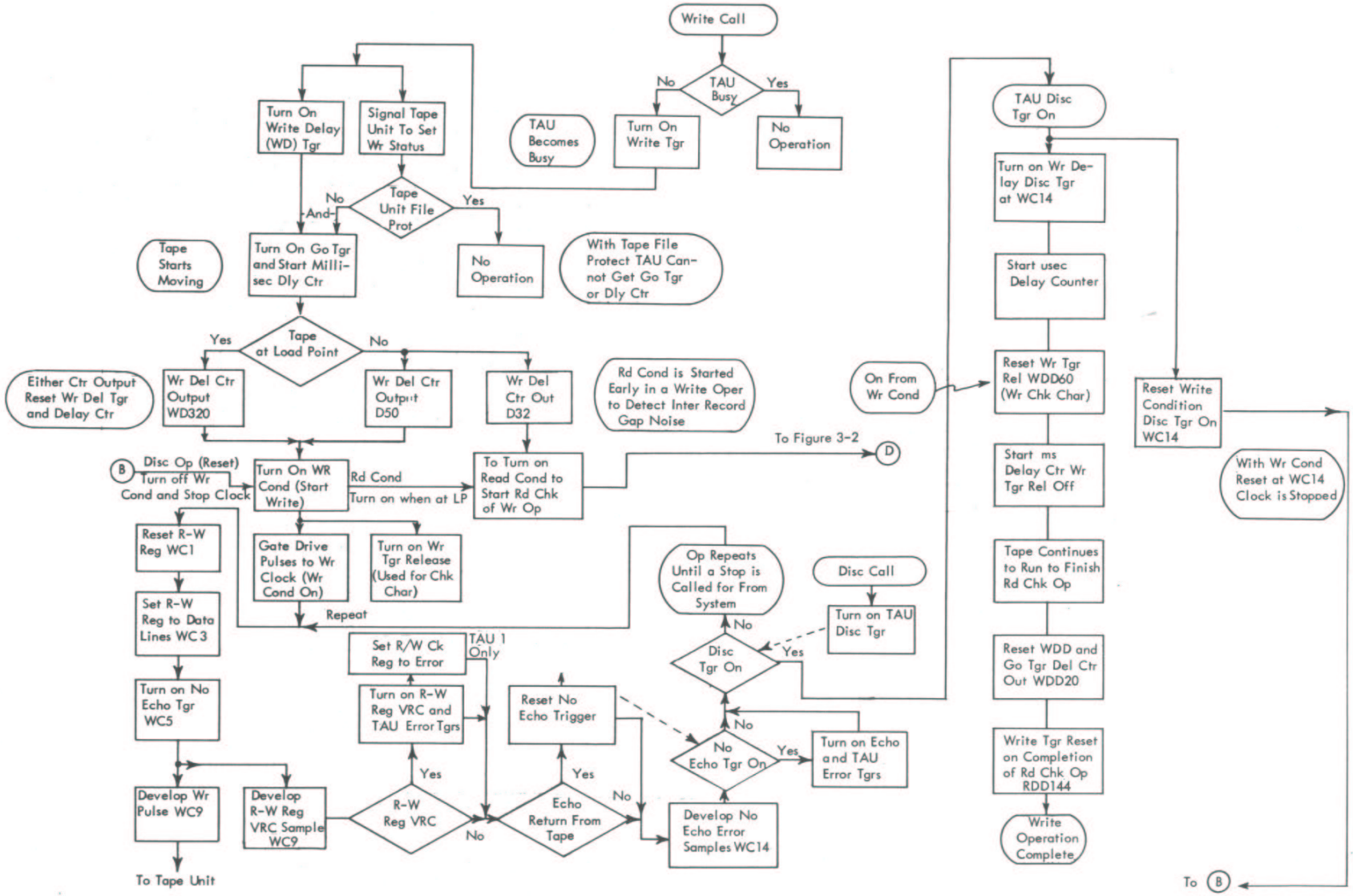


Figure 3-4. Write Operation

3.2.5 Backspace

The backspace operation is similar to a read operation, except that no data are transferred from tape to the system (Figure 3-5). When backspace call is initiated and the tape unit is in read status, TAU conditions the tape unit to move backward for one record and return to forward status. If the tape unit is in write status, TAU causes the tape to move forward and erase noise created by changing from read to write status (Figure 3-9).

Characters set into the read register during backspace start the read clock, which resets at the end of each character. When the end-of-record is reached, the read clock initiates action to stop backspacing and to set the tape unit in forward status.

The read-write register and TAU error checking circuits are not conditioned on during this operation, because no data are made available to the system.

3.2.6 Rewind

Two rewind operations are possible in TAU: normal rewind and rewind-unload (Figure 3-5). In the normal rewind operation, a rewind call signal conditions the TAU rewind trigger on. This trigger output is sent to the tape unit and initiates a rewind operation. When the tape unit goes into rewind status, the TAU rewind trigger is reset, completing the operation.

For the rewind-unload operation, TAU initiates the tape unload function by setting tape unit control circuits to unload tape from the vacuum columns after the rewind operation is completed.

3.3 Timing, Control and Data Flow

3.3.1 Timing Sequence Charts

Figures 3-6 through 3-10 show timing relationships for each major function of TAU. Each function is shown on a separate chart which lists all lines required to perform the function in proper sequence.

3.3.2 Tape Unit Control Lines

Major control lines between TAU and the tape unit are shown in Figures 3-11 and 3-12.

3.3.3 Read and Write Data Flow

Main data flow paths through TAU (reading and writing), which connect the tape unit to the arithmetic processing unit, are shown in Figures 3-13 through 3-15.

3.3.4 Delay Counter and Clocks

Delay counter control timing is shown in Figure 3-16. The delay counter consists of ten binary triggers. The DC1 trigger is driven directly from the oscillator, forming the drive timing and sample pulse. The next four triggers are driven in parallel by a 400-nanosecond timing pulse. The remaining five are driven in series by the output of the preceding trigger.

Delay counter timings control tape motion and data flow timings; they are named and numbered according to the gate lines, or the sum of counts added in the gating circuits. (See Figures 3-17 and 3-18.)

READ CLOCK

The read clock consists of four binary triggers separated by 400-nanosecond delay lines. These four triggers are driven in parallel by a 400-nanosecond timing pulse derived from a clamped oscillator and a single-shot. The trigger outputs are used as read timing control (Figures 3-19 and 3-20).

WRITE CLOCK

The write clock consists of four binary triggers separated by 400-nanosecond delay lines. These triggers are driven in parallel by a 400-nanosecond timing pulse from a crystal oscillator. The trigger outputs are used as write timing control. (See Figures 3-21 and 3-22.)

3.4 Power Supply Requirements

DC VOLTAGES (ALL ±4%)	MAXIMUM CURRENT (AMPERES)
+ 6 (marginal check)	1.68
−12 (marginal check)	1.33
+ 6	2.38
−12	4.00
− 6	1.19
+30	.10
−36	.22

Power-on reset is effective until all voltages have stabilized in the control and tape units.

All voltages should be regulated simultaneously.

Noise should not exceed 150 millivolts, measured between any two points on the power distribution buses within TAU panels.

3.5 TAU Oscillators

Ten different oscillator cards (Figure 3-23) are necessary to supply timing reference pulses for six different character rates. Only three oscillators are used at one time with a given tape unit and density.

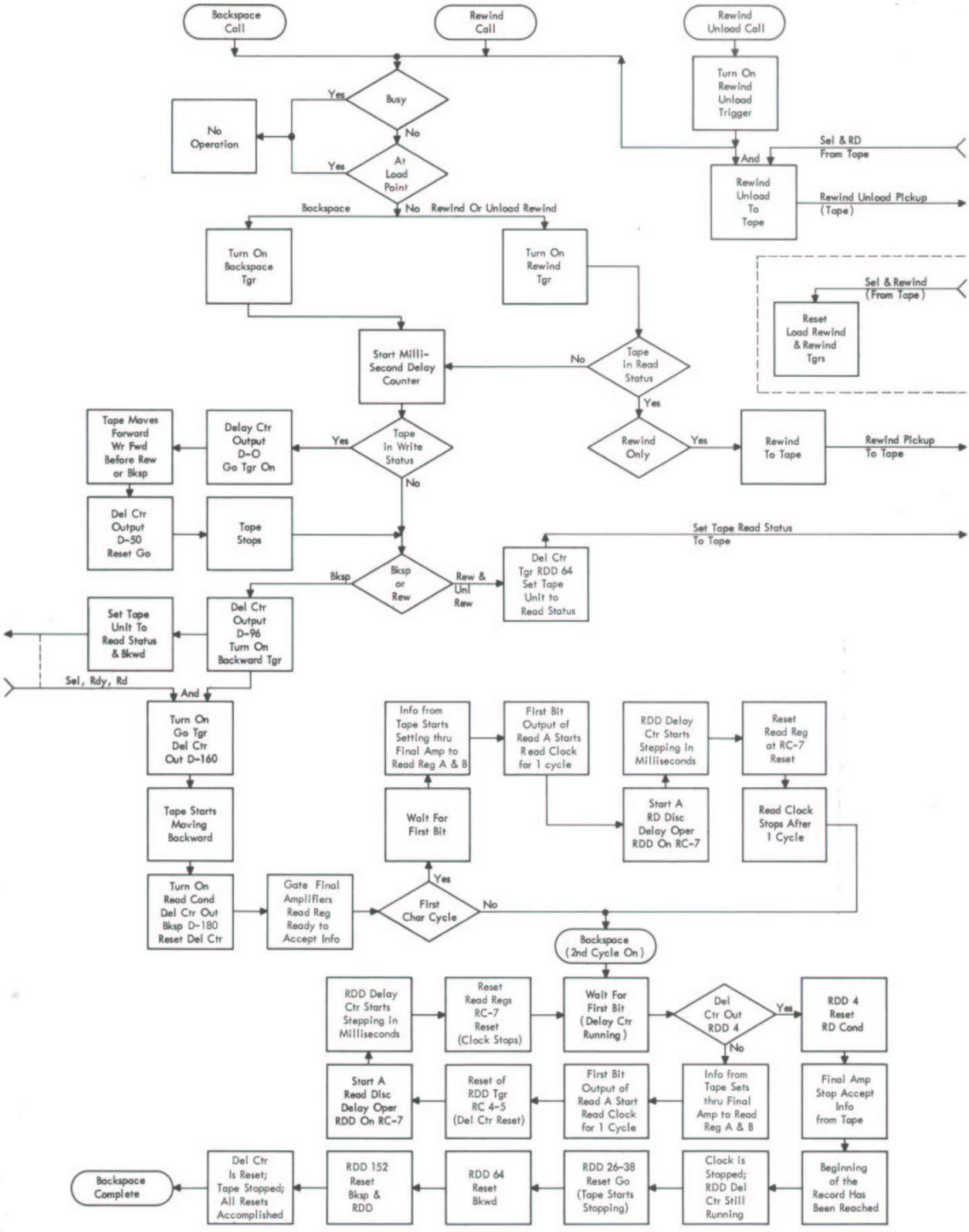


Figure 3-5. Backspace Call Logic

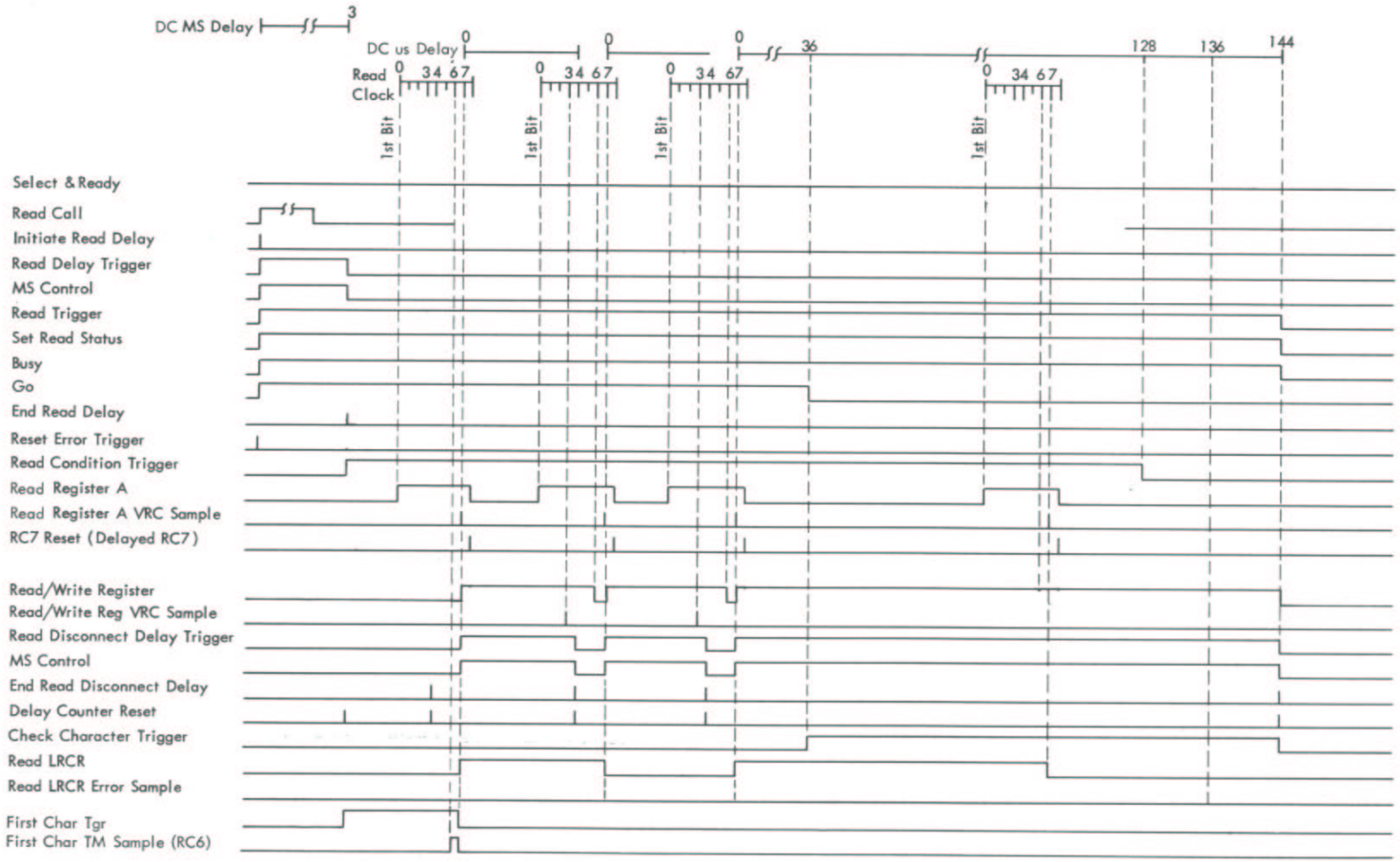


Figure 3-6. Read Timing

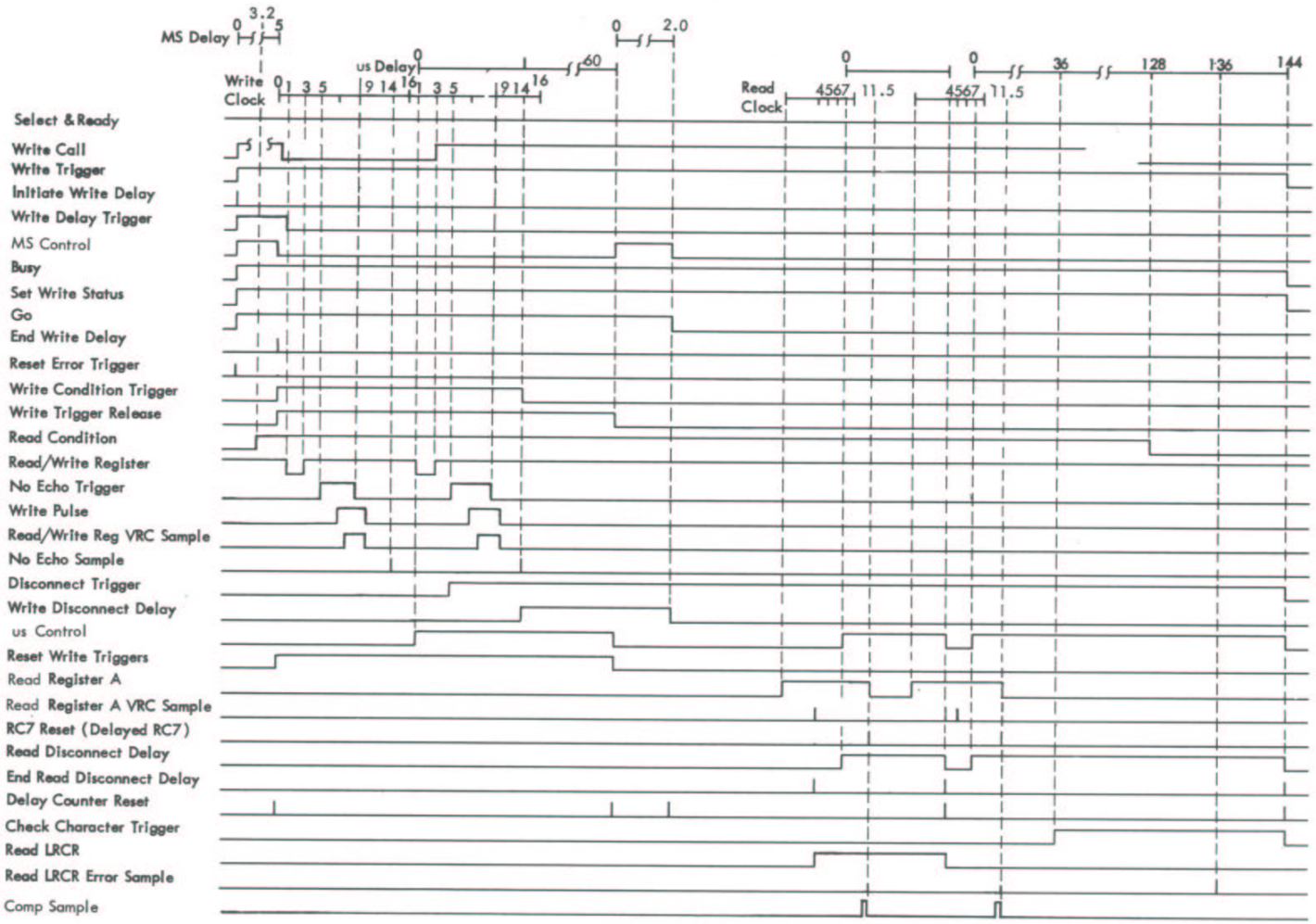


Figure 3-7. Write Timing

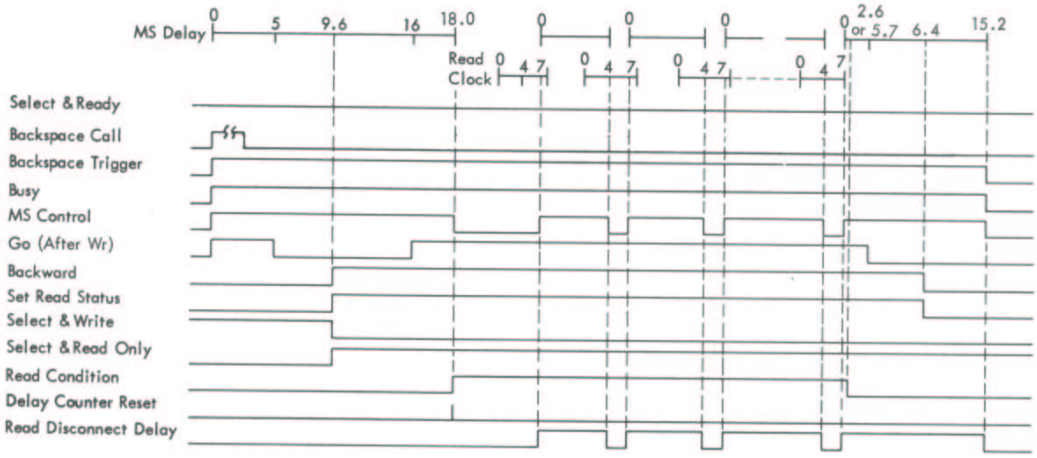


Figure 3-8. Backspace Timing

Delay	TAU/Ckt Affected	Delay Count	729 II	729 IV
Write Fwd	Go Tgr	D0 to D50	7ms	5.0ms
Bkwd Set Delay	Bkwd Tgr	D50 to D90	6.9ms	4.6ms
Set Rd Status	Set Rd Status	D96	-----	-----
Fwd to Bkwd	Go Tgr	D96 to D160	9.6ms	6.4ms
Bkwd Rd Dly	Rd Cond Tgr	D160 to Bksp 180	3.0ms	2.0ms
Bkwd Stop Dly	Go Tgr	RDD 0 to RDD 26 or 38	5.7ms	2.6ms
Bkwd Reset Dly	Bkwd Tgr	R DD 26 or 38 to RDD 64	3.9ms	3.8ms
Bkwd to Fwd	Bksp Tgr (Busy)	RDD64 to RDD152	12.9ms	8.8ms

Figure 3-9. Backspace after Write Timing Sequence

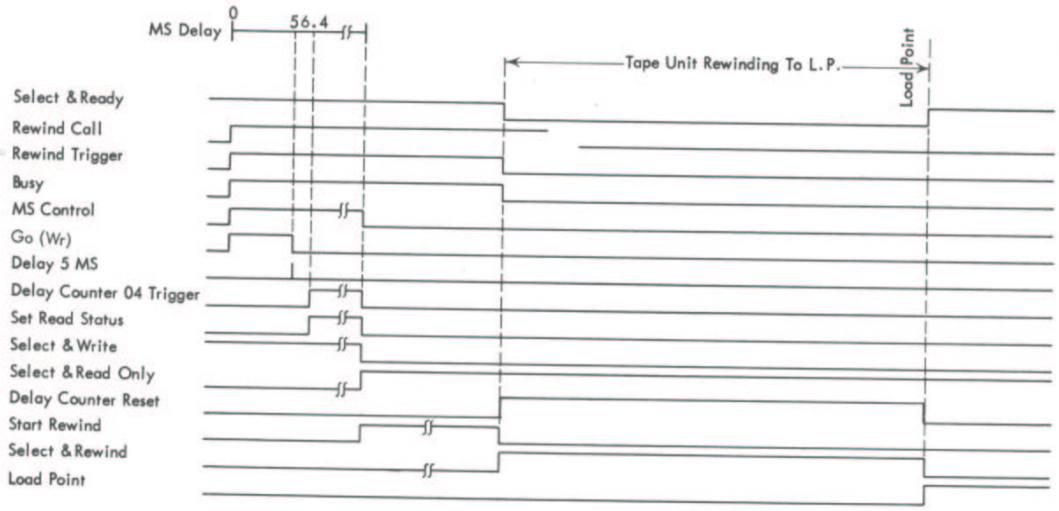


Figure 3-10. Rewind Timing

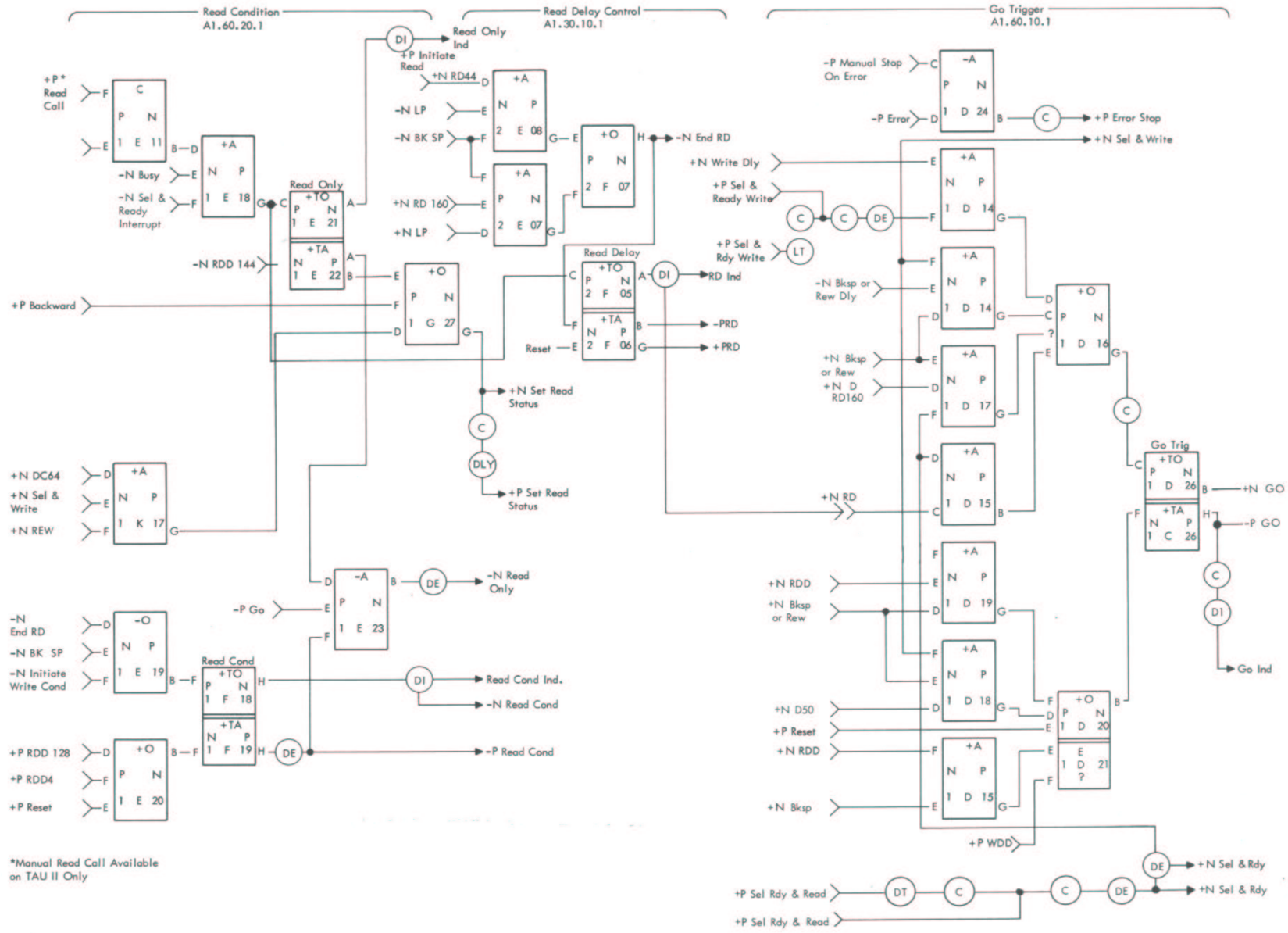


Figure 3-11. Read Tape Control Lines

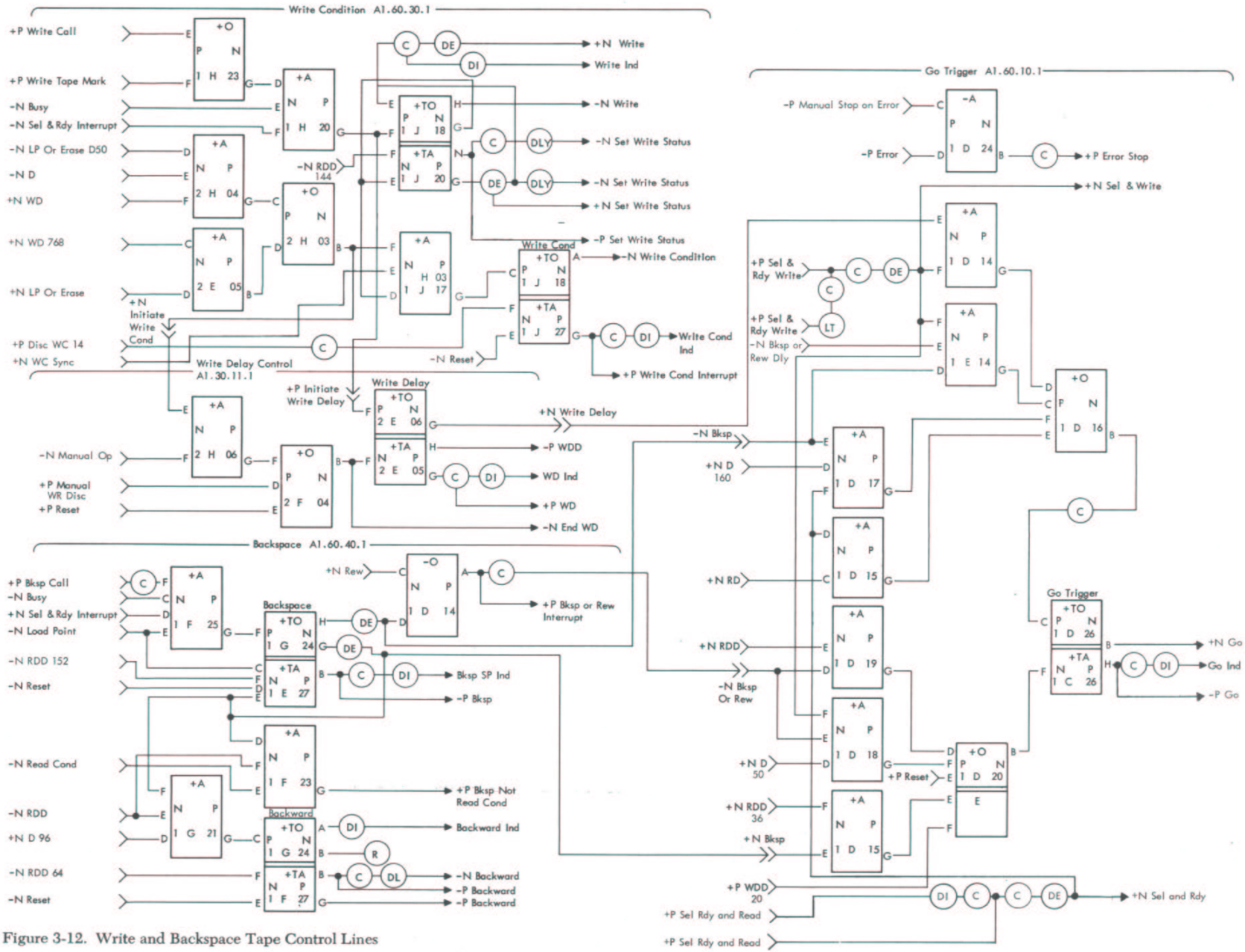


Figure 3-12. Write and Backspace Tape Control Lines

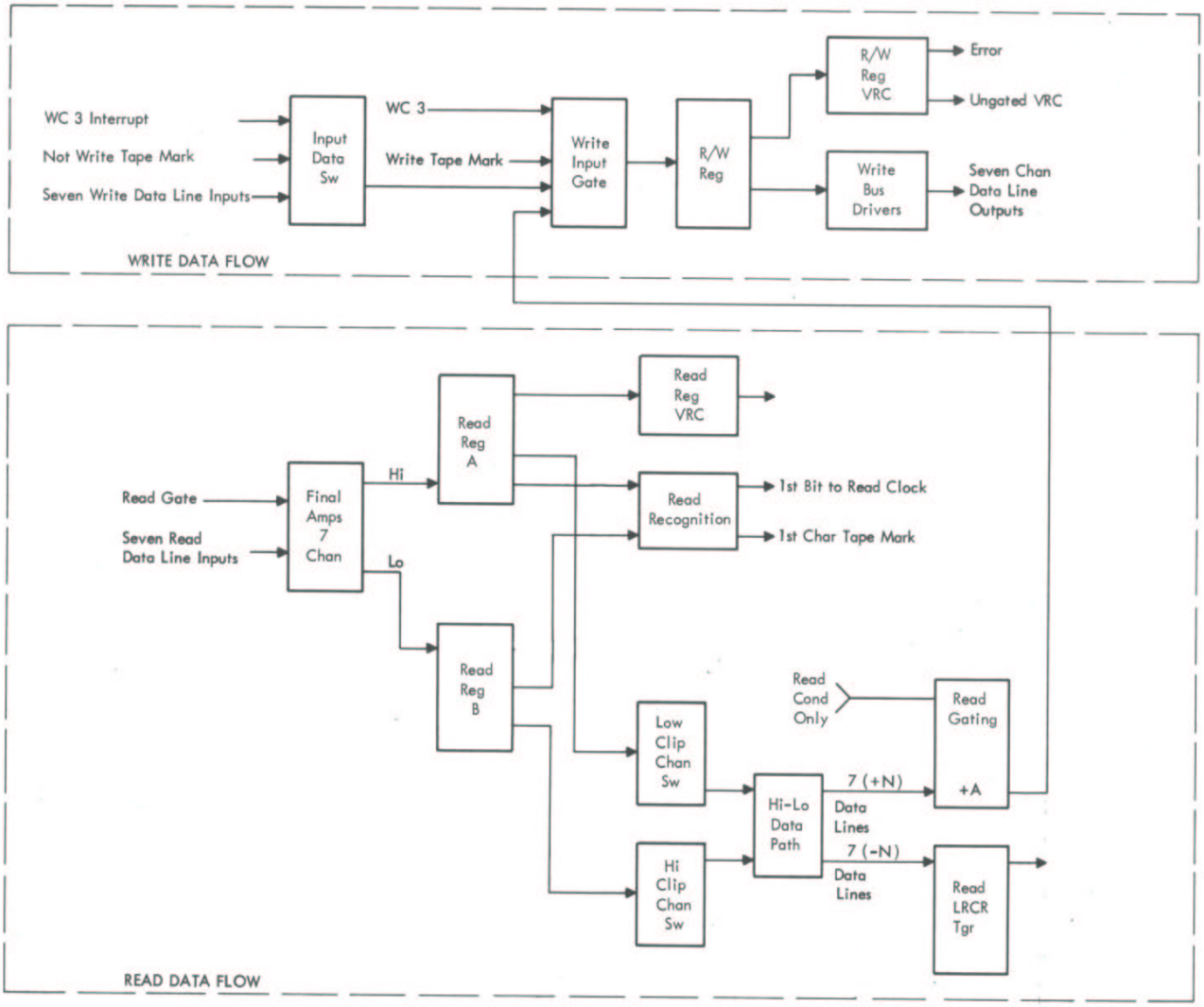


Figure 3-13. Read and Write Data Flow

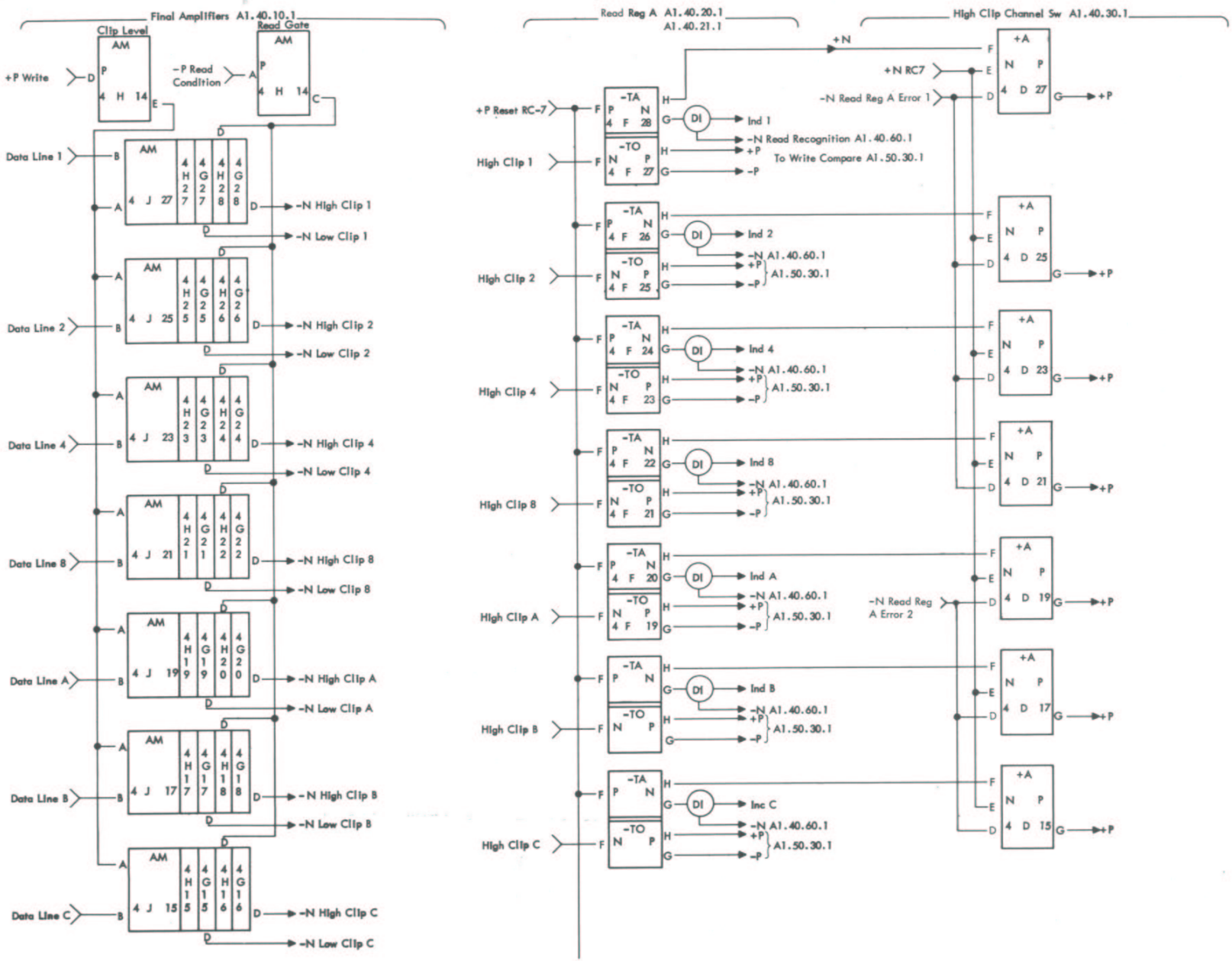


Figure 3-14A. Read Data Flow

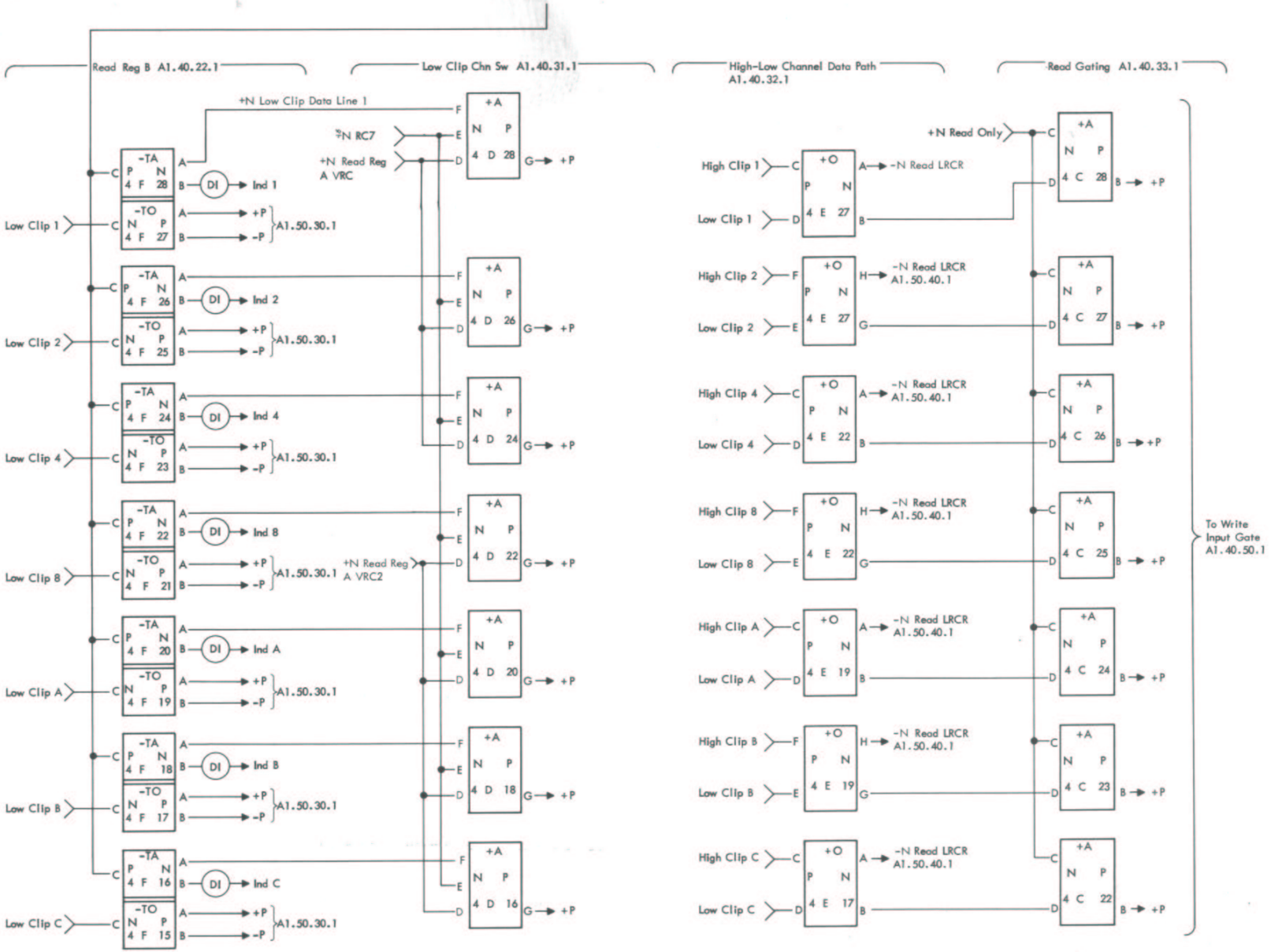


Figure 3-14B. Read Data Flow

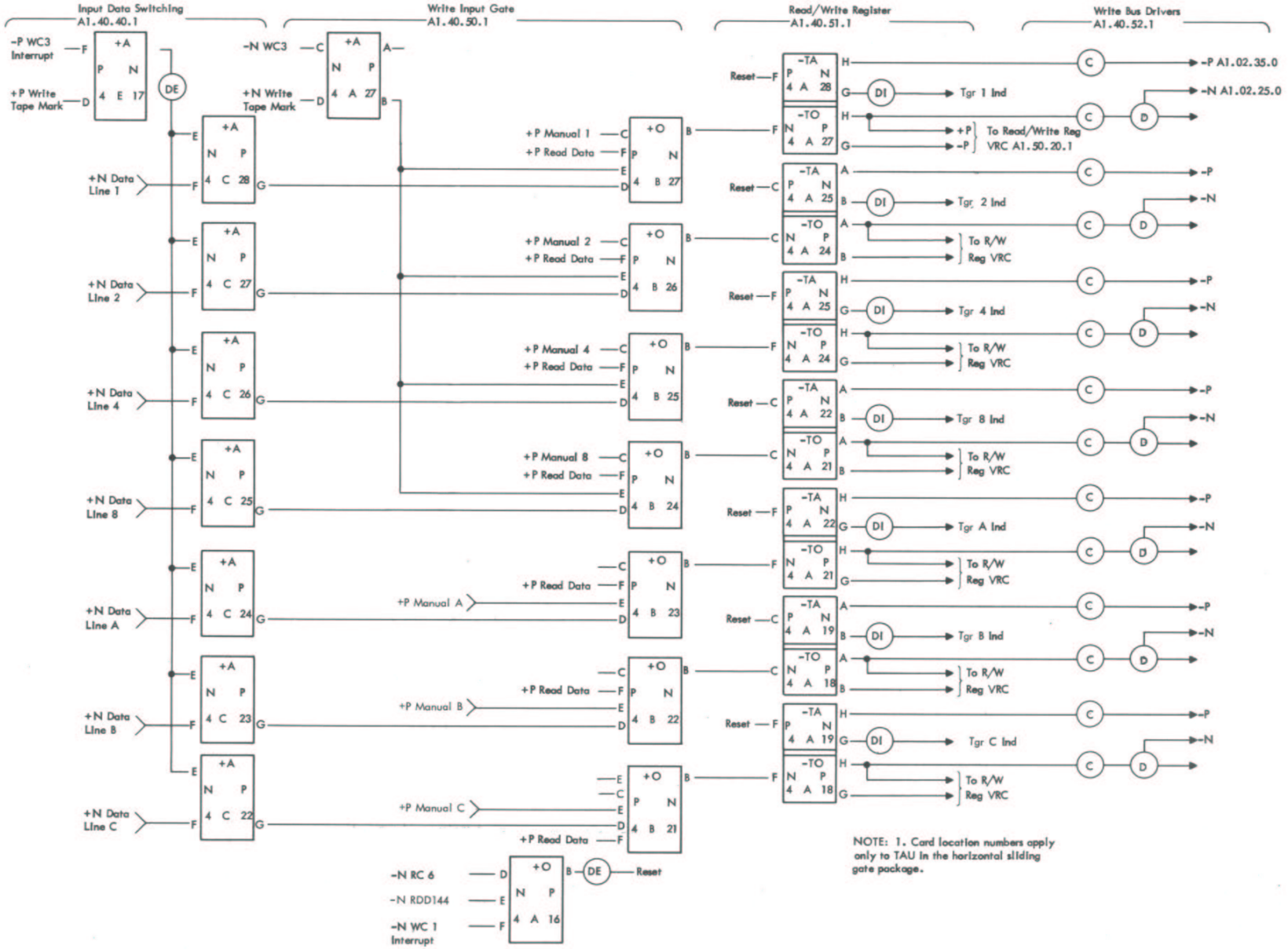


Figure 3-15. Write Data Flow

Microsecond Control: Read Disconnect (RDD) and Write Disconnect Delay (WDD)				
	729 II		729 IV	
	Low Density	High Density	Low Density	High Density
RDD 36	150 usec	54 usec	100 usec	36.0 usec
RDD 128	532 usec	192 usec	355 usec	128.0 usec
RDD 144	600 usec	216 usec	400 usec	144.0 usec
WDD 60	250 usec	90 usec	166 usec	60.0 usec

All delay counter microsecond timings are ± 1% (except RDD 36 which is 2%) and are measured in respect to the turn-on of RDD or WDD triggers in microsecond control.

Millisecond Control: Read Delay (RD), Write Delay (WD, RDD, WDD), and Backspace Timings			
	729 II	729 IV	Tolerance
RDD 4	0.6 ms	0.4 ms	± 12%
RDD 26 + RDD 38	5.7 ms + 1%	2.6 ms	± 2%
RDD 30*	4.5 ms	3.0 ms	± 2%
RDD 64	9.6 ms	6.4 ms	± 1%
RDD 152	22.5 ms	15.2 ms	± 1%
WDD 20	3.0 ms	2.0 ms	± 3%
RD 30	4.5 ms	3.0 ms	± 2%
RD 160	24.0 ms	16.0 ms	± 1%
WD 52	7.8 ms	5.2 ms	± 1%
WD 80	10.0 ms	8.0 ms	± 1%
WD 768	115.0 ms	76.8 ms	± 1%
D 50	7.5 ms	5.0 ms	± 1%
D 96	14.4 ms	9.6 ms	± 1%
D 160	24.0 ms	16.0 ms	± 1%
Backspace 180	27.0 ms	18.0 ms	± 1%
*TAU II Only			

All delay counter millisecond timings are measured in respect to the rise of millisecond control gate, except backspace timings, which are referenced to the rise of RDD

Figure 3-16. Microsecond and Millisecond Control

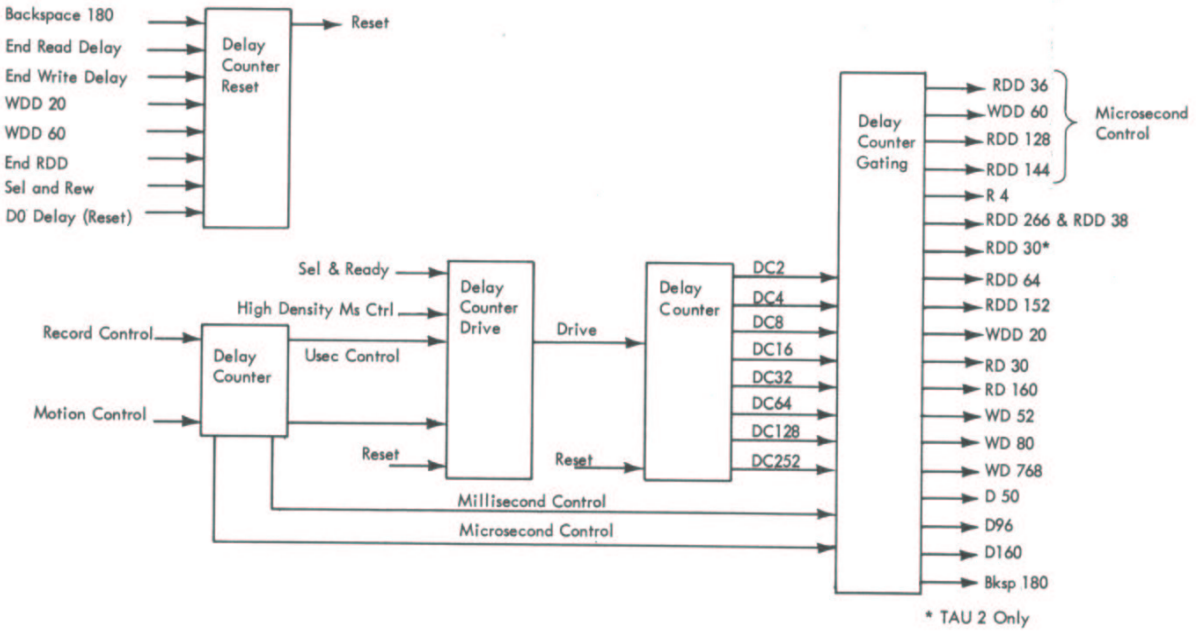


Figure 3-17. Delay Counter

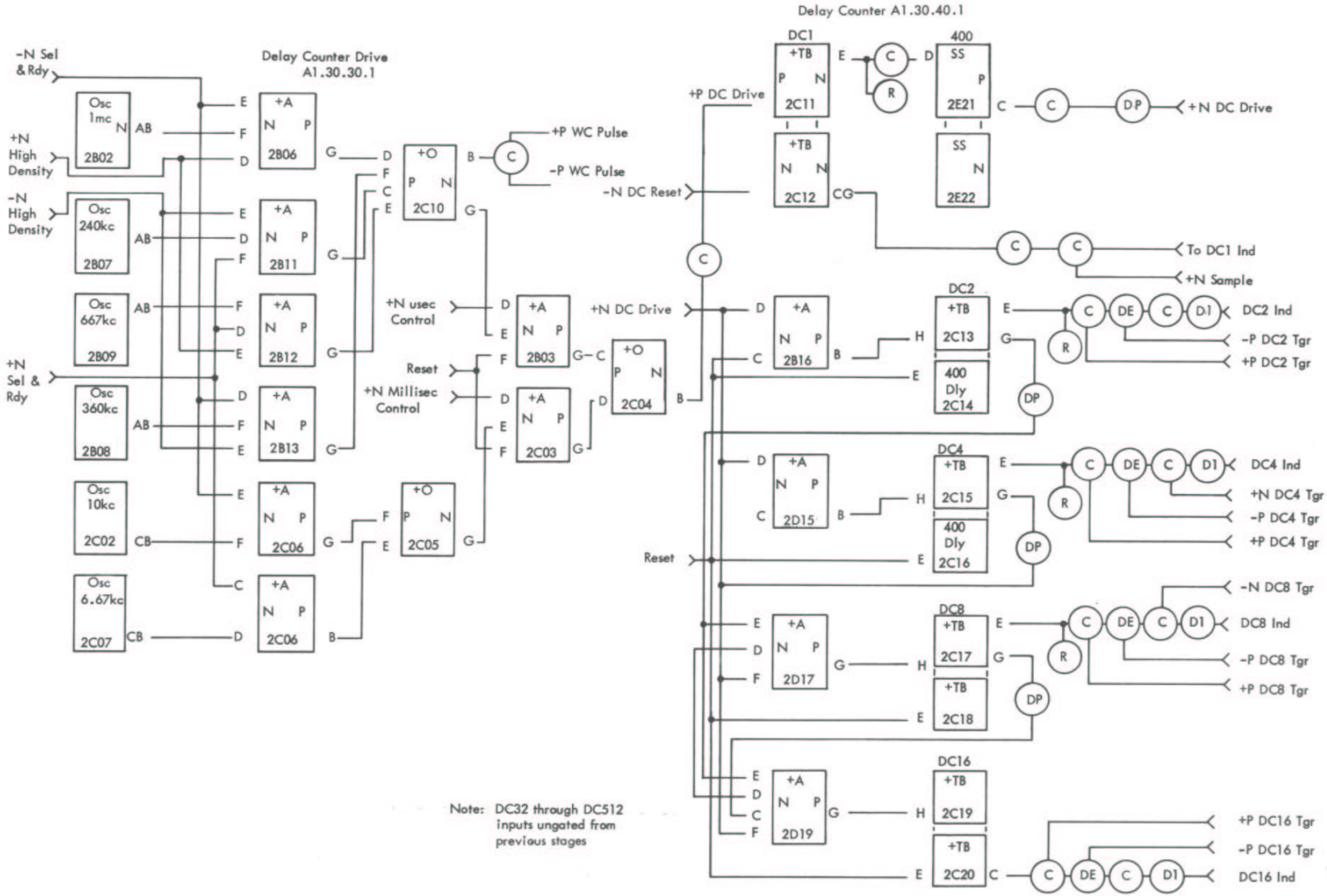


Figure 3-18. Delay Counter

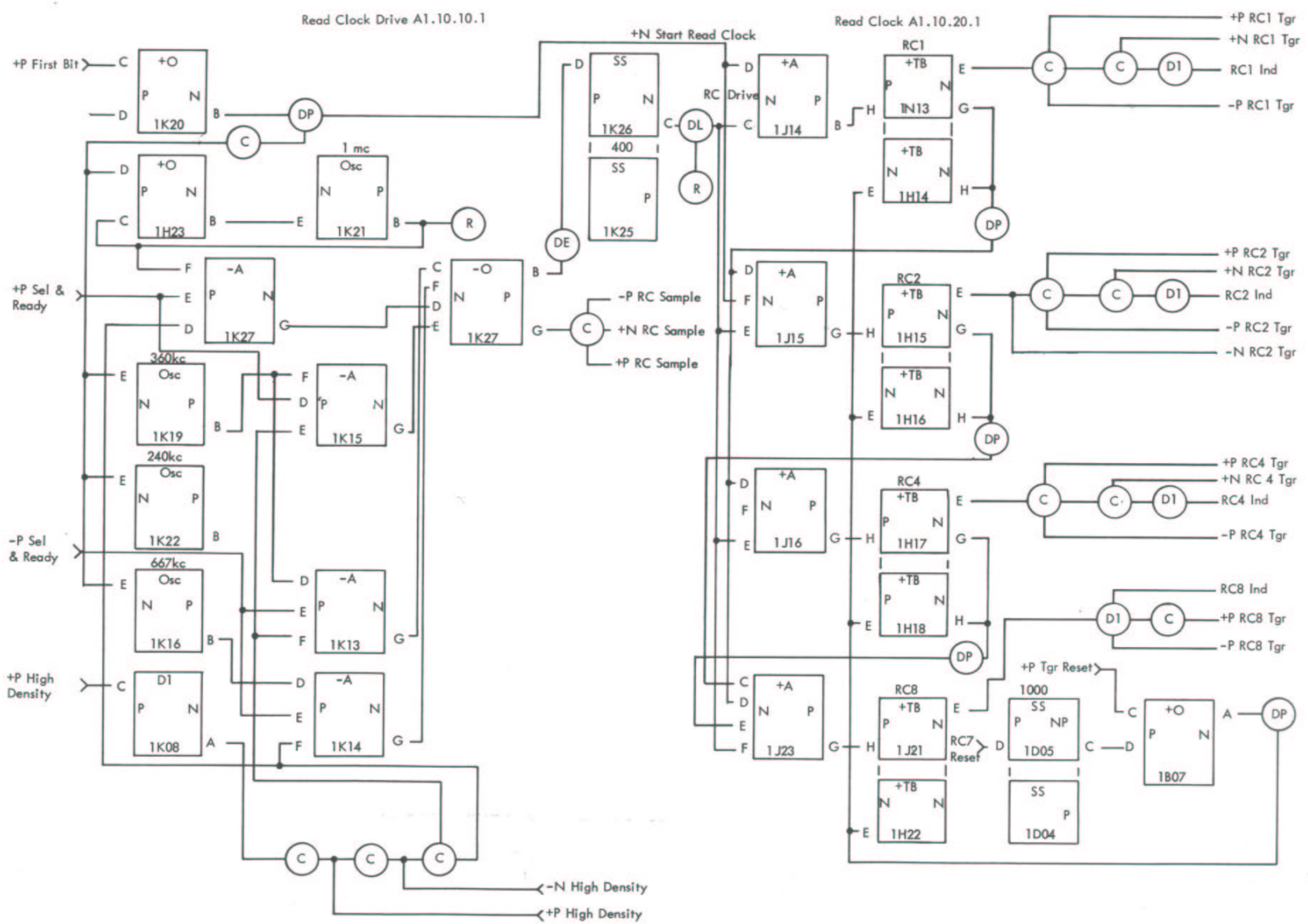


Figure 3-19A. Read Clock

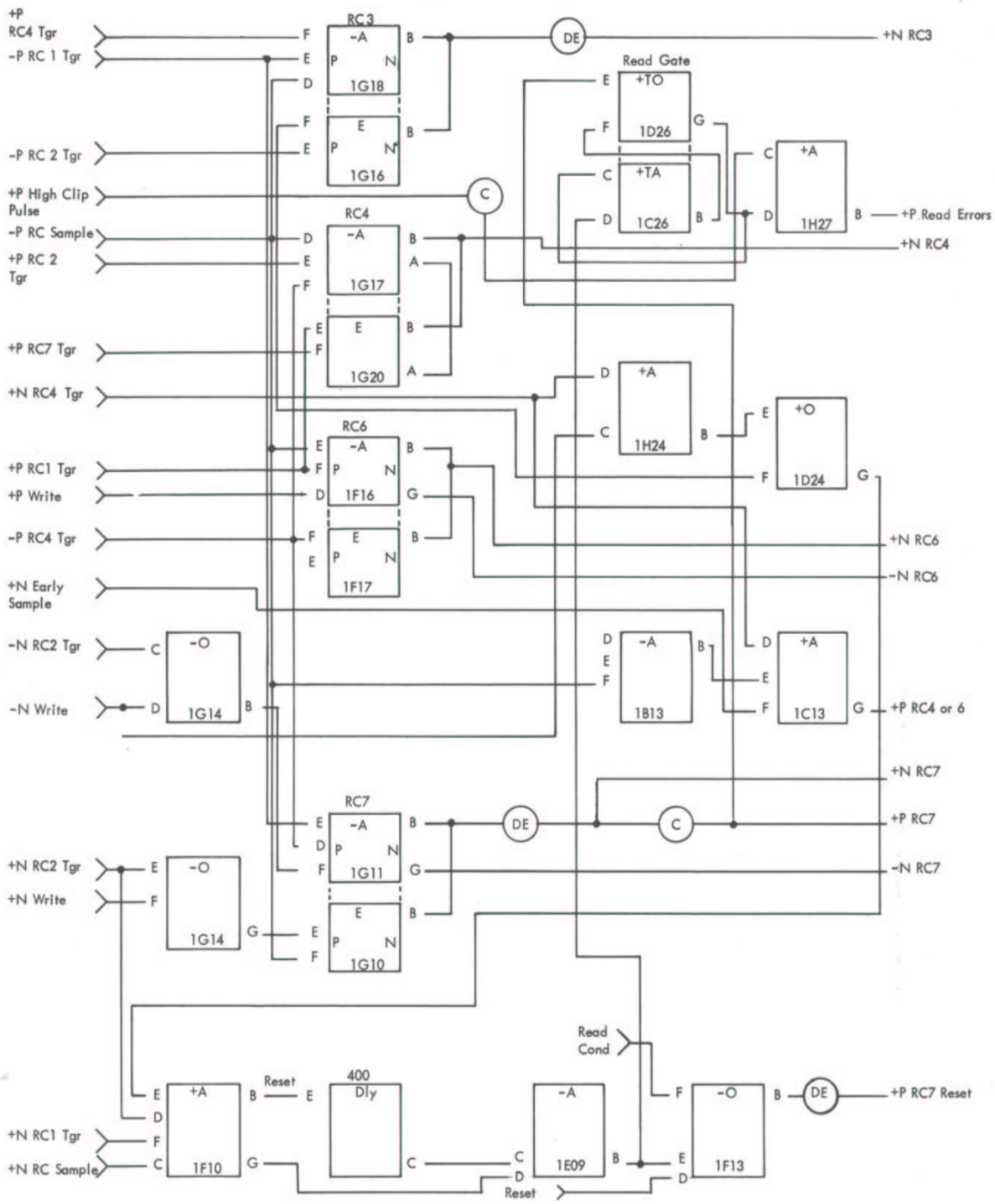
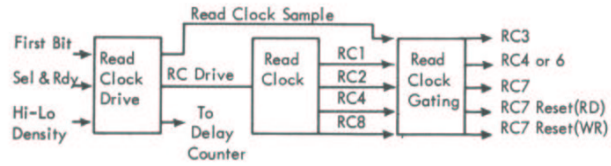


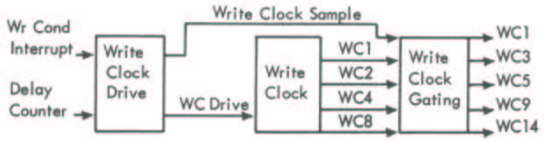
Figure 3-19B. Read Clock



Tape Unit Type and Bit Density Timing (Microseconds)				
Read Clock Output	729 II Low	729 II High	729 IV Low	729 IV High
RC1	4.5	1.8	3.1	1.3
RC3	12.8	4.8	8.6	3.3
RC4	16.9	6.3	11.4	4.3
RC7 (WR)	21.1	7.8	14.1	5.3
RC6	25.3	9.3	17.0	6.3
RC7	29.5	10.8	19.7	7.3
RC7 Reset (RD)	29.8	11.2	20.1	7.7
RC7 Reset (WR)	48.1	17.0	32.3	11.8

All read clock timings are ± 5% and are measured with respect to the rise of the first bit line.

Figure 3-20. Read Clock



Tape Unit Type and Bit Density Timing (Microseconds)				
Read Clock Output	729 II Low	729 II High	729 IV Low	729 IV High
WC1	Ref	Ref	Ref	Ref
WC3	8.32	3.0	5.56	2.0
WC5	16.6	6.0	11.1	4.0
WC9	31.5	11.5	21.1	7.75
WC14	54.1	19.5	36.1	13.0
WC1	66.6	24.0	44.5	16.0

All write clock timing pulses are ± 1% with respect to the turn-off of the WC1 timing pulse.

Figure 3-21. Write Clock

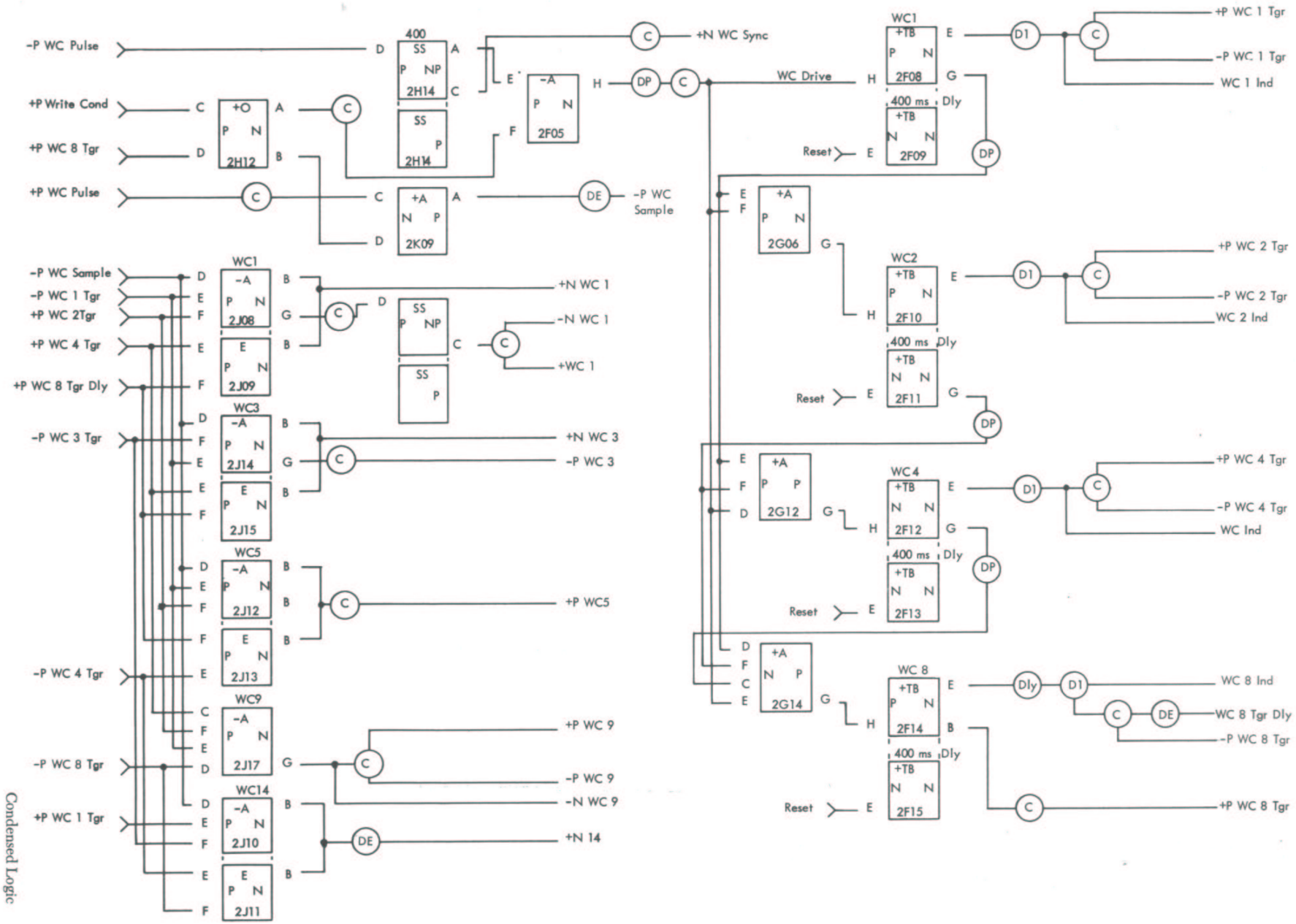


Figure 3-22. Write Clock

Oscillator	Type	Tape Unit	Frequency Accuracy	Function
6.7 KC	Crystal	729 II	± 1%	Delay counter millisecond control
10.0 KC	Crystal	729 IV	± 1%	Delay counter millisecond control
240 KC	Crystal	729 II	± 1%	Delay counter usec control and write clock 200 bits/inch
240 KC	Clamped	729 II	± 5%	Read clock drive 200 bits/inch
360 KC	Crystal	729 IV	± 1%	Delay counter usec control and write clock 200 bits/inch
360 KC	Clamped	729 IV	± 5%	Read clock drive 200 bits/inch
667 KC	Crystal	729 II	± 1%	Delay counter usec and write clock drive at 555.5 bits/inch
667 KC	Clamped	729 II	± 5%	Read clock drive 555 .5 bits/inch
1 MC	Crystal	729 IV	± 1%	Delay counter usec control and write clock drive at 555.5 bits/inch
1 MC	Clamped	729 IV	± 5%	Read clock drive at 555.5 bits/inch

Figure 3-23. TAU Oscillators

4.1 Read Waveforms

Figure 4-1 shows waveforms for read bus, mixer outputs, peak detector, shapers, RDD trigger, delay counter reset trigger, and delay counter microsecond control.

4.2 Write Waveforms

Figure 4-2 shows waveforms for first bit, skew gate, A vertical redundancy sample, compare check, skew sample, skew gate, RDD 36, RDD 128, and RDD 144.

4.3 Marginal Checking

Two variable voltages, supplied to TAU from an external power supply, are available for marginal checking and may be used to troubleshoot intermittent troubles. These voltages are +6v DC, variable from +3.5v to +8.5v, and −12v DC, variable from −9.5v to −14.5v. They were selected for marginal checking because of their general use throughout TAU circuitry as bias voltages that establish operation points and, to some extent, determine transistor reverse current (IC_o). In many cases, intermittent troubles can be made to fail by causing them to operate at either maximum or minimum bias voltage limit. These failures can then be located by conventional troubleshooting methods.

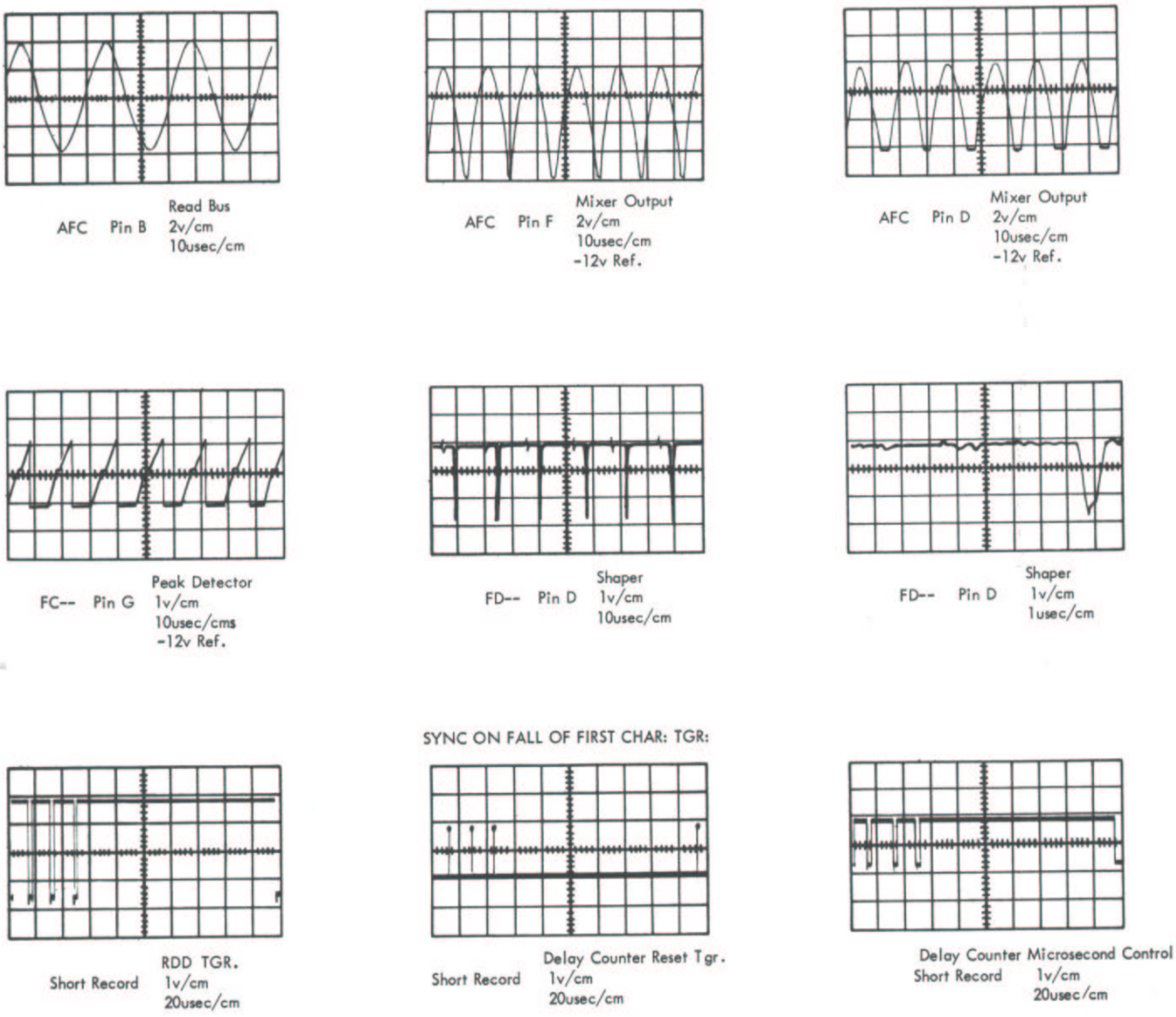
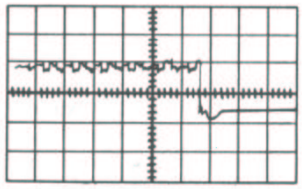
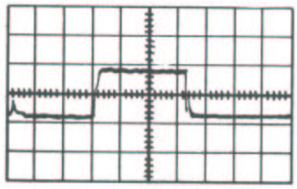


Figure 4-1. Read Waveforms, 729 IV High Density

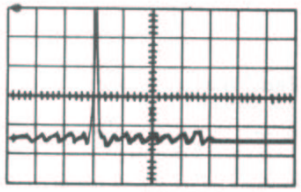
SYNC ON FIRST BIT



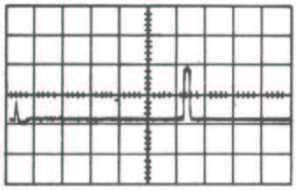
First Bit
1v/cm
2usec/cm



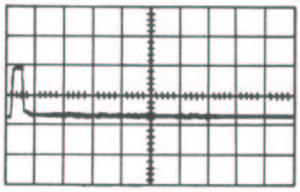
Skew Gate
1v/cm
2usec/cm



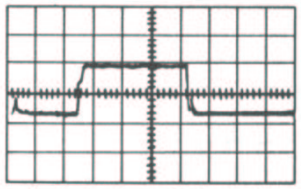
"A" VRC Sample
RC7
1v/cm
2usec/cm



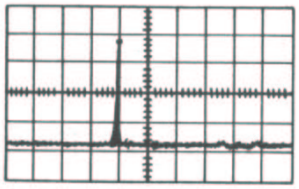
Compare Check Sample
(RC7 Reset)
1v/cm
2usec/cm



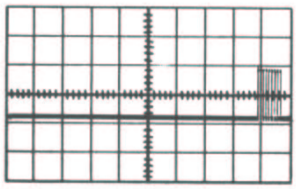
Skew Gate Sample
(Hi Clip)
1v/cm
2usec/cm



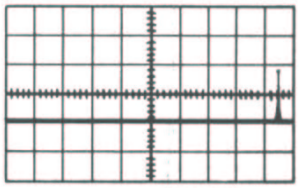
Skew Gate
(With Early Sample On)
1v/cm
1usec/cm



Short Record
RDD 36
1v/cm
20usec/cm



Short Record
RDD 128
1v/cm
20usec/cm



Short Record
RDD 144
1v/cm
20usec/cm

Figure 4-2. Write Waveforms, 729 IV High Density

Contents

5.1 Machine Locations ... 35
5.1.1 TAU I ... 35
5.1.2 TAU II ... 35
5.1.3 Printed Wiring Cards ... 37
5.1.4 Laminar Bus ... 37
5.1.5 Card Receptacles ... 37
5.1.6 T-Connector (Terminal Block) ... 37
5.1.7 Edge-Cabling Connectors ... 37
5.1.8 Horizontal Edge Connector ... 37
5.2 Troubleshooting Hints ... 38
5.3 Other Aids ... 38
5.3.1 TAU I, Input and Output Signal Description ... 38
5.3.2 Control Unit Signals ... 38
5.3.3 Indicator Driver Signals ... 41
5.4 Special Circuits ... 41
5.4.1 TAU Final Amplifier ... 41
5.4.2 Clipping Level Circuits ... 41
5.4.3 P Type Trigger Circuit ... 41
5.5 Differences Between TAU I and TAU II ... 44
5.5.1 Packaging Differences ... 44
5.5.2 Logic Differences ... 44
5.6 TAU Applications ... 44

5.1 Machine Locations

5.1.1 TAU I

TAU I incorporates SMS cards, printed wiring, and the horizontal sliding gate module II assembly. There are two slides per module, each containing two gates. Each gate contains four card chassis frames or panels. TAU circuitry occupies three panels of one card chassis frame (Figures 5-1 through 5-4).

Each card chassis frame accommodates up to 280 card positions in ten rows of 28 card positions. All spaces are not used to contain printed wiring cards; some are used as edge connector receptacles for interconnecting horizontally adjacent panels, while others are used for signal input and output connector receptacles.

5.1.2 TAU II

TAU II incorporates SMS cards, printed wiring, and the vertical swinging gate assembly. There are eight gates per module and two modules per assembly. Any four panels of either module can contain TAU (Figures 5-5 and 5-6).

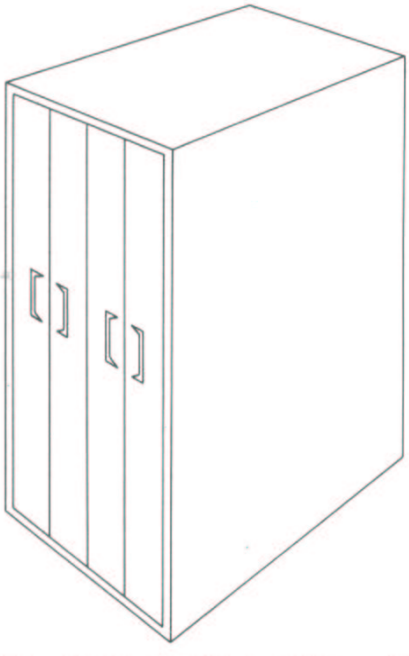


Figure 5-1. Module II Horizontal Gate and Frame

Figure 5-2 . Module II Card Chassis (TAU I)

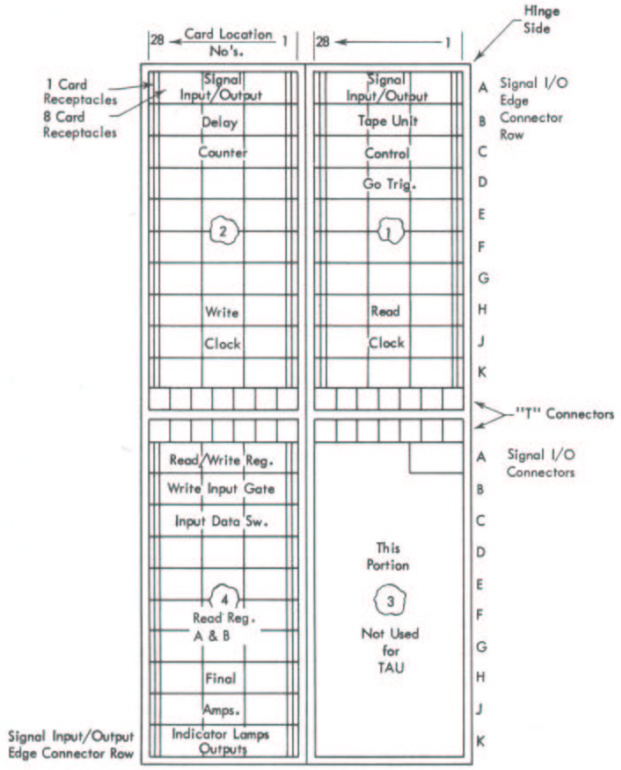


Figure 5-3. TAU I Card Chassis

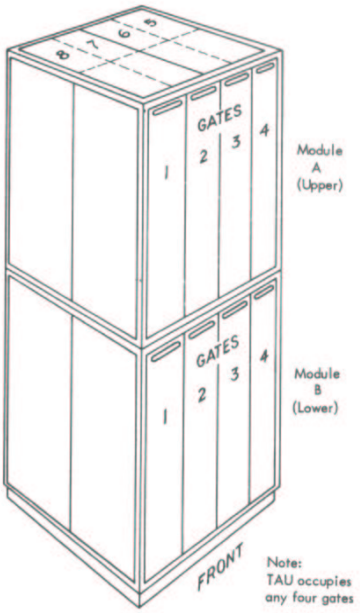


Figure 5-5. TAU II Vertical Swinging Gate

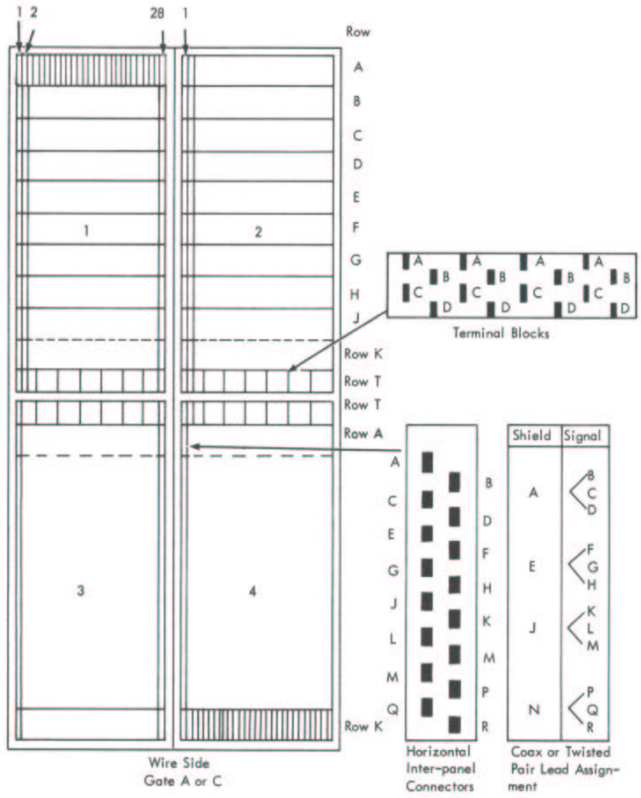


Figure 5-4. TAU I Card Chassis (Rear View Showing Laminar Bus)

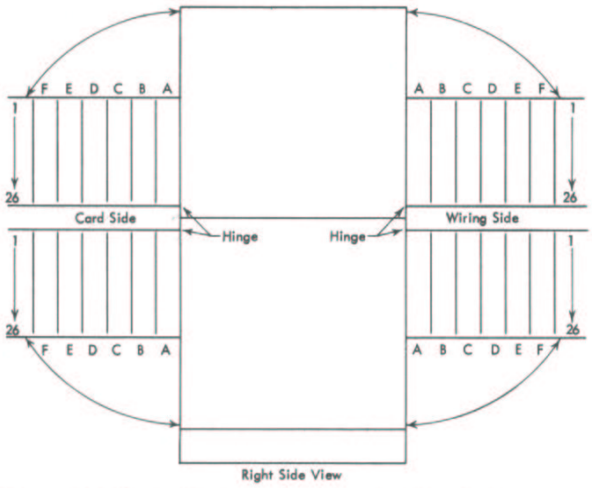


Figure 5-6. Vertical Swinging Gate Location Numbering

5.1.3 *Printed Wiring Cards*

There are two basic types of printed wiring cards; one has a program cap, and the other does not. A transistor card can be modified by the program cap to form several circuit configurations. The program cap is two conductor rails prepunched to form 15 legs with one common base. These legs can be punched out to form various jumpering conditions. Figure 5-7 shows a card using the program cap.

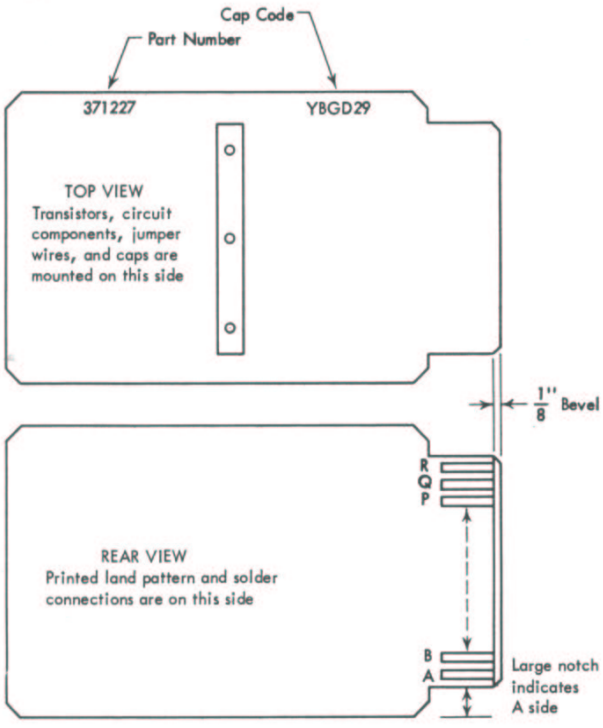


Figure 5-7. Printed Wiring Card

5.1.4 *Laminar Bus*

The laminar bus distributes power from the main power supply to all TAU transistor cards. It consists of eight layers of copper strips, each separated by MYLAR* insulation. This laminated assembly is mounted on a plastic board which has sixteen terminals for connecting spring crimped connectors from the laminar bus to the card receptacles.

5.1.5 *Card Receptacles*

Card receptacles are used in single units or groups of eight (Figure 5-8). Two single receptacles, three 8-card receptacles, and two more single-card receptacles constitute a full row of 28 card receptacles in a TAU chassis. Figure 5-8 shows receptacles in the card chassis frames.

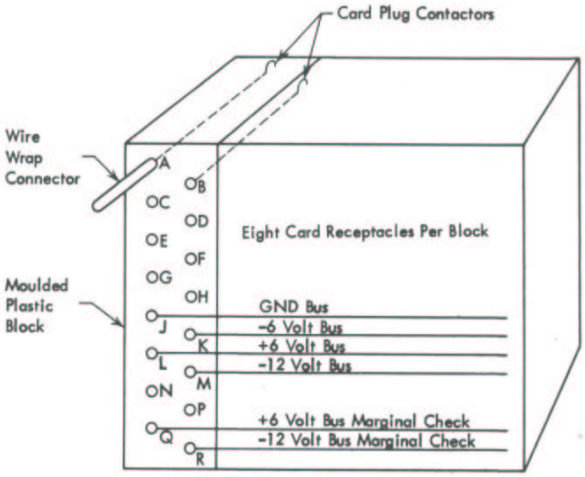


Figure 5-8. Eight-Card Receptacle, Rear View

5.1.6 *T-Connector (Terminal Block)*

The T-connector is a 16-pin terminal block positioned between panels 1 and 3, and panels 2 and 4 in the TAU frame. These terminal blocks are tie points for inter-connecting signal wires between vertically adjacent panels. There are 28 T-connectors per gate.

5.1.7 *Edge-Cabling Connectors*

Edge-cabling connectors along the top and bottom of the TAU card chassis frame provide input and output signal connections to and from TAU. These connectors are identical and interchangeable with card receptacles.

5.1.8 *Horizontal Edge Connector*

This connector is identical to the single-card receptacle and is used to provide a receptacle for card jumper plugs which interconnect both signal and power lines between horizontally adjacent panel 1 and panel 2.

*Trademark of E. I. du Pont de Nemours & Co. (Inc.)

5.2 Troubleshooting Hints

1. More than one of each logic circuit is available in TAU and, probably, no two will exhibit the same trouble symptom at any given time. Therefore, printed wiring cards operating properly may be used for service aids as follows:
   a. Compare the oscilloscope waveforms of a suspected defective circuit with the waveform of a known operating, identical circuit.
   b. Substitute printed wiring cards operating properly for identical cards suspected of defects.
2. Isolate the suspected circuit from its input and output connections whenever possible. This helps to determine if the circuit is defective or if the trouble symptoms are caused externally by defective input or output of circuits.

5.3 Other Aids

5.3.1 TAU I, Input and Output Signal Description

See Figures 5-9 and 5-10. All TAU input signal lines, except the read bus, from the tape unit must be −N or +P current switching levels terminated in a transmission line terminator. This circuit is a dot OR function with one to ten tape unit capacity, provided total external cabling does not exceed 100 feet.

All TAU output signals to the tape unit are −N or +P current switching levels driven by a transmission line driver. These output lines can drive one to ten tape units if total external cabling does not exceed 100 feet.

TAU read bus inputs are voltage level with nominal signal values of 8.5 to 8.8 volts peak-to-peak (low density, while writing).

5.3.2 Control Unit Signals (Figures 5-11 and 5-12)

Signals from the control unit to TAU are current switching level with less than 3600 picofarad shunt capacitance.

LEVEL	NAME		SYSTEMS PAGE
P	HIGH DENSITY		001 A1.10.10.1
8V.	PP	1 DATA LINE	002 A1.40.10.1
8V.	PP	1 DATA LINE	003 A1.40.10.1
8V.	PP	2 DATA LINE	004 A1.40.10.1
8V.	PP	2 DATA LINE	005 A1.40.10.1
8V.	PP	4 DATA LINE	006 A1.40.10.1
8V.	PP	4 DATA LINE	007 A1.40.10.1
8V.	PP	8 DATA LINE	008 A1.40.10.1
8V.	PP	8 DATA LINE	009 A1.40.10.1
8V.	PP	A DATA LINE	010 A1.40.10.1
8V.	PP	A DATA LINE	011 A1.40.10.1
8V.	PP	B DATA LINE	012 A1.40.10.1
8V.	PP	B DATA LINE	013 A1.40.10.1
8V.	PP	C DATA LINE	014 A1.40.10.1
8V.	PP	C DATA LINE	015 A1.40.10.1
-N	WR ECHO		016 A1.50.50.1
-N	WRITE ECHO		017 A1.50.50.1
P	SEL 0 RDY	MII	018 A1.60.01.1
P	SEL 0 RDY M4		019 A1.60.01.1
P	SEL 0 RDY M2		020 A1.60.01.1
P	SEL 0 LP		021 A1.60.01.1
P	SEL RDY 0	WRITE	022 A1.60.10.1
P	SEL RDY 0	READ	023 A1.60.10.1
-N	SEL 0 REW		024 A1.60.50.1
P	SEL 0 NOT LP		025 A1.60.60.1
-N	SEL 0 TI ON		026 A1.60.60.1
-N	SEL 0 TI OFF		027 A1.60.60.1

Figure 5-9. Inputs from Tape Unit to TAU I

Output signals from TAU to the control unit are current switching level and are capable of driving only one transistor base.

Interrupts (Figure 5-13) are available at the chassis edge connectors.

LEVEL	NAME		SYSTEMS PAGE
-N	WRITE BUS 1		001 A1.40.52.1
-N	WRITE BUS 2		002 A1.40.52.1
-N	WRITE BUS 4		003 A1.40.52.1
-N	WRITE BUS 8		004 A1.40.52.1
-N	WRITE BUS A		005 A1.40.52.1
-N	WRITE BUS B		006 A1.40.52.1
-N	WRITE BUS C		007 A1.40.52.1
P	GO		008 A1.60.10.1
P	SET READ	STATUS	009 A1.60.20.1
-N	SET WR	STATUS	010 A1.60.30.1
-N	RESET WRITE TGRS		011 A1.60.32.1
-N	WRITE PULSE		012 A1.60.32.1
-N	BACKWARD		013 A1.60.40.1
P	REWIND	UNLOAD	014 A1.60.50.1
-N	REWIND		015 A1.60.50.1
P	SET HI	DENSITY	016 A1.60.60.1
-N	SET LO	DENSITY	017 A1.60.60.1
P	TURN OFF TI		018 A1.60.60.1
-N	TURN ON TI		019 A1.60.60.1

Figure 5-10. Outputs from TAU I to Tape Unit

LEVEL	NAME		SYSTEMS PAGE
N	EARLY SAMPLE		001 A1.10.30.1
P	MANUAL WRITE DISC		002 A1.30.11.1
-N	MANUAL OP		003 A1.30.11.1
P	AMPLIFIER	BIAS	004 A1.40.10.1
N	1 DATA LINE		005 A1.40.40.1
N	2 DATA LINE		006 A1.40.40.1
N	4 DATA LINE		007 A1.40.40.1
N	8 DATA LINE		008 A1.40.40.1
N	A DATA LINE		009 A1.40.40.1
N	B DATA LINE		010 A1.40.40.1
N	C DATA LINE		011 A1.40.40.1
P	1 MANUAL		012 A1.40.50.1
P	2 MANUAL		013 A1.40.50.1
P	4 MANUAL		014 A1.40.50.1
P	8 MANUAL		015 A1.40.50.1
P	A MANUAL		016 A1.40.50.1
P	B MANUAL		017 A1.40.50.1
P	C MANUAL		018 A1.40.50.1
P	ODD RED CALL		019 A1.40.60.1
P	EVEN RED	CALL	020 A1.40.60.1
N	EARLY SAMPLE		021 A1.50.10.1
P	REG A ONLY		022 A1.50.10.1
P	REG B ONLY		023 A1.50.10.1
P	COMPARE	CHECK	024 A1.50.30.1
P	MANUAL	ERROR RESET	025 A1.50.50.1
P	SEL 0 RDY	MIV	026 A1.60.01.1
P	SEL RDY 0 RD		027 A1.60.10.1
P	SEL RDY 0 WR		028 A1.60.10.1
-P	MANUAL STOP ON ERROR		029 A1.60.10.1
P	READ CALL		030 A1.60.20.1
P	WRITE CALL		031 A1.60.30.1
P	W TM CALL		032 A1.60.31.1
P	ERASE CALL		033 A1.60.31.1
P	BKSP CALL		034 A1.60.40.1
P	DISC CALL		035 A1.60.50.1
P	MANUAL WRITE DISC		036 A1.60.50.1
P	REWIND CALL		037 A1.60.50.1
P	REW	UNLOAD CAL	038 A1.60.50.1
N	TURN OFF TI		039 A1.60.60.1
-P	TURN ON TI		040 A1.60.60.1
N	SET HI	DENSITY	041 A1.60.60.1
-P	SET LO	DENSITY	042 A1.60.60.1
P	MACHINE OR THERMAL	PWR ON RES INTERLOCK	043 A1.70.01.1 044 A1.70.01.1

Figure 5-11. Inputs from Control Unit to TAU I

		SYSTEMS PAGE
P	HIGH DENSITY	A1.10.10.1
N	RC 3	A1.10.30.1
-N	RC 6	A1.10.30.1
-N	RC 6	A1.10.30.1
-N	WC 1	A1.20.30.1
N	WC 14	A1.20.30.1
P	WC 5	A1.20.30.1
-P	WR PULSE	A1.20.30.1
N	WC 1	A1.20.30.1
-N	WC 9	A1.20.30.1
-P	RDD	A1.30.10.1
N	WDD	A1.30.11.1
P	WD	A1.30.11.1
-P	US SAMPLE	A1.30.20.1
-P	DC 8 TR	A1.30.41.1
-P	DC 16 TR	A1.30.41.1
-P	DC 32 TR	A1.30.42.1
-P	DC 64 TR	A1.30.42.1
-P	DC 128 TR	A1.30.42.1
P	DC 32 TR	A1.30.42.1
-N	RDD 144	A1.30.50.1
N	RDD 36	A1.30.50.1
P	RDD 128	A1.30.50.1
P	WDD 60	A1.30.50.1
N	RDD 136	A1.30.50.1
N	RDD 136	A1.30.50.1
-N	RDD 144 ONLY	A1.30.50.1
-N	WDD 20	A1.30.51.1
P	RDD 152	A1.30.52.1
P	RDD 152	A1.30.52.1
N	WD 52	A1.30.52.1
N	WD 80	A1.30.52.1
N	WD 768	A1.30.53.1
-N	2 DATA LINE	A1.40.51.1
-N	8 DATA LINE	A1.40.51.1
-N	B DATA LINE	A1.40.51.1
-N	1 DATA LINE	A1.40.51.1
-N	4 DATA LINE	A1.40.51.1

		SYSTEMS PAGE
-N	A DATA LINE	A1.40.51.1
-N	C DATA LINE	A1.40.51.1
-P	1 DATA LINE	A1.40.52.1
-P	2 DATA LINE	A1.40.52.1
-P	4 DATA LINE	A1.40.52.1
-P	8 DATA LINE	A1.40.52.1
-P	A DATA LINE	A1.40.52.1
-P	B DATA LINE	A1.40.52.1
-P	C DATA LINE	A1.40.52.1
-N	CHECK CHAR	A1.40.60.1
P	FIRST CHAR TAPEMARK	A1.40.60.1
P	ERROR	A1.50.50.1
P	ERROR	A1.50.50.1
-P	ECHO ERROR	A1.50.50.1
-N	LOAD POINT	A1.60.01.1
-N	BUSY	A1.60.01.1
P	SEL 0 LD PT	A1.60.01.1
P	SEL 0 LD PT	A1.60.01.1
N	GO	A1.60.10.1
-N	GO RESET	A1.60.10.1
N	SET READ STATUS	A1.60.20.1
-P	READ COND	A1.60.20.1
-N	WRITE TR	A1.60.30.1
-P	SET WR STATUS	A1.60.30.1
P	ERASE	A1.60.31.1
P	ERASE	A1.60.31.1
-P	RESET WRITE TGRS	A1.60.32.1
P	BACKSPACE	A1.60.40.1
-P	BACKWARD	A1.60.40.1
-P	REWIND READ	A1.60.50.1
-P	REWIND	A1.60.50.1
N	REWIND UNLOAD	A1.60.50.1
-P	SEL 0 REW	A1.60.50.1
P	SEL 0 NOT LP	A1.60.60.1
-N	SEL 0 TI ON	A1.60.60.1
-N	SEL 0 TI OFF	A1.60.60.1
THERMAL	INTERLOCK	A1.70.01.1
P	TR RESET	A1.70.01.1

Figure 5-12. Outputs from TAU I to Control Unit

LEVEL	NAME	SYSTEMS PAGES
N	RC 7	A1.10.30.1
P	WRITE COND	A1.20.10.1
-P	WC 3	A1.20.30.1
P	P RDD TR RESET	A1.30.10.1
P	RDD TR RESET	A1.30.10.1
N	RC 7	A1.30.10.1
P	RDD 144 DLY	A1.30.10.1
P	RDD TR RESET	A1.30.10.1
P	RDD TR RESET	A1.30.10.1
P	RDD 144 DLY	A1.30.50.1
P	RDD 144	A1.30.50.1
P	RDD 4	A1.30.51.1
-P	WC 3	A1.40.40.1
P	UNGATED VRC	A1.50.20.1

LEVEL	NAME	SYSTEMS PAGE
P	UNGATED VRC	A1.50.20.1
P	READ LRCR ERROR	A1.50.40.1
N	ERROR	A1.50.50.1
P	READ LRCR ERROR	A1.50.50.1
N	ERROR	A1.50.50.1
N	SEL 0 READY	A1.60.01.1
P	BKSP OR REW	A1.60.01.1
N	SEL 0 READY	A1.60.20.1
P	RDD 4	A1.60.20.1
P	WRITE COND	A1.60.30.1
N	SEL 0 READY	A1.60.30.1
N	SEL 0 READY	A1.60.31.1
P	BKSP OR REW	A1.60.40.1
N	SEL 0 READY	A1.60.40.1
N	SEL 0 READY	A1.60.50.1

Figure 5-13. Interrupts, Input and Output

LEVEL NAME	SYSTEMS PAGES
WC 8 IND	A1.20.20.1
WC 1 IND	A1.20.20.1
WC 2 IND	A1.20.20.1
WC 4 IND	A1.20.20.1
WD IND	A1.30.11.1
WDD IND	A1.30.11.1
READ REG A 1 IND	A1.40.20.1
READ REG A 2 IND	A1.40.20.1
READ REG A 4 IND	A1.40.20.1
READ REG A 8 IND	A1.40.20.1
READ REG A A IND	A1.40.21.1
READ REG A B IND	A1.40.21.1
READ REG A C IND	A1.40.21.1
READ REG B 1 IND	A1.40.22.1
READ REG B 2 IND	A1.40.22.1
READ REG B 4 IND	A1.40.22.1
READ REG B 8 IND	A1.40.22.1
READ REG B A IND	A1.40.22.1
READ REG B B IND	A1.40.22.1
READ REG B C IND	A1.40.22.1
READ REG A ERROR IND	A1.50.10.1
COMPARE ERROR IND	A1.50.30.1
RW REG VRC IND	A1.50.50.1
DC 512 IND	A1.60.01.1
READ ONLY IND	A1.60.20.1
READ COND IND	A1.60.20.1

LEVEL NAME	SYSTEMS PAGES
WRITE IND	A1.60.30.1
WRITE COND IND	A1.60.30.1
WRITE TM IND	A1.60.31.1
ERASE IND	A1.60.31.1
WR TR REL IND	A1.60.32.1
RC 1 IND	A1.10.20.1
RC 2 IND	A1.10.20.1
RC 4 IND	A1.10.20.1
RDD IND	A1.30.10.1
RD IND	A1.30.10.1
DC RESET IND	A1.30.31.1
DC 1 IND	A1.30.40.1
DC 2 IND	A1.30.41.1
DC 4 IND	A1.30.41.1
DC 8 IND	A1.30.41.1
DC 16 IND	A1.30.41.1
DC 32 IND	A1.30.42.1
DC 64 IND	A1.30.42.1
DC 128 IND	A1.30.42.1
DC 256 IND	A1.30.42.1
TR 2 IND	A1.40.51.1
TR 8 IND	A1.40.51.1
TR B IND	A1.40.51.1
TR 1 IND	A1.40.51.1
TR 4 IND	A1.40.51.1
TR A IND	A1.40.51.1
TR C IND	A1.40.51.1

LEVEL NAME	SYSTEMS PAGES
CHECK CHAR IND	A1.40.60.1
ODD RED IND	A1.40.60.1
FIRST CHAR IND	A1.40.60.1
READ LRCR 4 IND	A1.50.41.1
READ LRCR A IND	A1.50.41.1
READ LRCR C IND	A1.50.41.1
READ LRCR 2 IND	A1.50.41.1
READ LRCR 8 IND	A1.50.41.1
READ LRCR 1 IND	A1.50.41.1
READ LRCR B IND	A1.50.41.1
ERROR TR IND	A1.50.50.1
ECHO ERROR IND	A1.50.50.1
NO ECHO IND	A1.50.50.1
RW CHECK REG 2 DATA LINE	A1.50.51.1
RW CHECK REG 8 DATA LINE	A1.50.51.1
RW CHECK REG B DATA LINE	A1.50.51.1
RW CHECK REG 1 DATA LINE	A1.50.51.1
RW CHECK REG 4 DATA LINE	A1.50.51.1
RW CHECK REG A DATA LINE	A1.50.51.1
RW CHECK REG C DATA LINE	A1.50.51.1
LOAD POINT IND	A1.60.01.1
GO IND	A1.60.10.1
BACKSPACE IND	A1.60.40.1
BACKWARD IND	A1.60.40.1
DISCONNECT IND	A1.60.50.1
REW IND	A1.60.50.1
REW UNLOAD IND	A1.60.50.1

Figure 5-14. Indicators

Backspace Trigger	A1.60.40.1
Backward Trigger	A1.60.40.1
Busy	A1.60.01.1
Check Char	A1.40.60.1
Delay Counter DC1	A1.30.40.1
Delay Counter DC2, 4, 8, 16	A1.30.41.1
Delay Counter DC32, 64, 128, 256	A1.30.42.1
Delay Counter Drive 1MC, 240KC, 667KC, 360KC 10KC, 6.67KC	A1.30.30.1
Delay Counter Gating D.O., RDD36, WDD60, RDD128, 136, 144	A1.30.50.1
Delay Counter Gating D50, WDD20, RDD4, 26-38	A1.30.51.1
Delay Counter Gating WD52, 80, RDD64, 152, D96	A1.30.52.1
Delay Counter Gating D160, RD160, BKSP180, WD768	A1.30.53.1
Delay Counter Reset	A1.30.31.1
Delay Counter Speed Control	A1.30.20.1
Delay Counter 512 Trigger	A1.60.01.1
Disconnect Trigger	A1.60.50.1
Echo Error	A1.50.50.1
Erase Trigger	A1.60.31.1
Error Trigger	A1.50.50.1
Final Amp	A1.40.10.1
First Bit	A1.40.60.1
First Character	A1.40.60.1
Go Trigger	A1.60.10.1
High Clip Channel Switching	A1.40.30.1
High Low Channel Data Path	A1.40.32.1
Input Data Switching	A1.40.40.1
Load Point Trigger	A1.60.01.1
Low Clip Channel Switching	A1.40.31.1
Man-Pow On Reset-Ther Interlock	A1.70.01.1
No Echo Trigger	A1.50.50.1
Odd Red	A1.40.60.1
Read A Error Trigger	A1.50.10.1
Read Clock RC1, 2, 4, 8	A1.10.20.1
Read Clock Drive 1MC, 360KC, 240KC, 667KC osc	A1.10.10.1
Read Clock Gating RC3, 4, 6, 7, and 7 Reset	A1.10.30.1
Read Cond Trigger	A1.60.20.1
Read Delay Trigger	A1.30.10.1
Read Disc Delay Trigger	A1.30.10.1
Read Gate	A1.40.10.1
Read Gating (Data)	A1.40.33.1
Read LRCR 1, 2, 4, 8, A, B, C Triggers	A1.50.40.1
Read LRCR Indicators	A1.50.41.1
Read Only Trigger	A1.60.20.1
Read Reg A1, 2, 4, 8 Triggers	A1.40.20.1
Read Reg AA, B, C Triggers	A1.40.21.1
Read Reg A VRC	A1.50.10.1
Read Reg B1, 2, 4, 8, A, B, C Triggers	A1.40.22.1
Rewind Trigger	A1.60.50.1
Rewind Unload Trigger	A1.60.50.1
R-W Check Reg (1, 2, 4, 8, A, B, C)	A1.50.51.1
R-W Register (1, 2, 4, 8, A, B, C) Triggers	A1.40.51.1
R-W Reg VRC	A1.50.20.1
R-W Reg VRC Trigger	A1.50.50.1
Sel and Ready	A1.60.01.1
Skew Error Trigger	A1.50.50.1
Skew Gate	A1.10.30.1
Tape Mark	A1.40.60.1
TU Lines	A1.60.60.1
Write Bus Drivers	A1.40.52.1
Write Clock WC1, 2, 4, 8	A1.20.20.1
Write Clock Drive	A1.20.10.1
Write Clock Gating WC1, 3, 5, 9, 14	A1.20.30.1
Write Compare	A1.50.30.1
Write Compare	A1.50.31.1
Write Condition Trigger	A1.60.30.1
Write Delay Control	A1.30.11.1
Write Delay Trigger	A1.30.11.1
Write Disc Delay Trigger	A1.30.11.1
Write Input Gate (Data)	A1.40.50.1
Write Pulse	A1.60.32.1
Write TM Trigger	A1.60.31.1
Write Trigger	A1.60.30.1
Write Trigger Rel	A1.60.32.1

Figure 5-15. ALD Index

5.3.3 Indicator Driver Signals (Figure 5-14)

The −N indicator driver circuits on all 18 TAU triggers use incandescent indicator circuits. Therefore, the customer engineering test panel for TAU must contain incandescent lamps to display triggers. These lamps are for use with 10v at 15 milliamperes.

NOTE: For cross-referencing of Figures 5-9 through 5-14, an alphabetical ALD index is shown in Figure 5-15.

5.4 Special Circuits

5.4.1 TAU Final Amplifier

The basic TAU final amplifier (Figure 5-16) consists of three SMS cards. Each card serves a specific function in the chain of events between the read bus signal and the ultimate −N current mode pulse which sets the read register trigger.

To the basic final amplifier, two additional cards for each of the seven tracks are added to make the second channel of the dual-channel system. These are duplicates of two of the three basic cards. The first card is used to perform five functions (AFC).

1. Amplify the signal 2.2 to 2.4 times (transformer).
2. Provide two signals 180° out of phase (transformer).
3. Impress a DC bias to provide a noise clipping level (transformer plus external control cards).
4. Rectify out-of-phase signals to provide in-phase signals (first transistor stage, emitter followers).
5. Provide two outputs, one of which is impressed with additional noise clipping (high and low clipping channels).

The normal read signal input to this card is taken as eight volts peak-to-peak and all acceptance level percentages are based on this figure. The sine wave frequency range for operating conditions is 7.5 kc to 32 kc. This range of frequencies is designed to provide maximum reliability for operating 729 II and 729 IV tape units.

The noise clipping applied to the first card is provided by three external cards and can be varied through a wide range of values with wiring changes. However, engineering has established the optimum values, and until an official change notice is issued these values are fixed. The actual minimum acceptance level for each channel can be computed using the following formula:

$$\text{Acceptance min.} = \frac{\text{Total clipping} + 0.1\text{v}}{8\text{v}}$$

This clipping value is switched between read and write operations to the values given in the specifications.

The outputs of this card are identical to the half-wave of the input amplified twice.

The second card provides two functions for the final amplifier system (FC−−): (1) differentiation and clamping, and (2) amplification and integration.

The time constant of the differentiator is selected to provide a flat response over the range of frequencies mentioned. After the differentiation the negative portion of the signal is clamped out and the positive portion is amplified about 20 times and integrated in the emitter follower output stage. This output provides a signal that has a fall time coincident with the input peak and, as such, is an effective peak senser. The integration provides a sharp cut-off to frequencies above the band pass to protect the system from noise.

The third (FD−−) card provides two functions, DC sensing and pulse generation. The input circuit to this card is essentially a Schmidt trigger. The signal charges the integrator of the previous card from −12 volts toward −6v. This will turn the Schmidt trigger on when the signal rises to about −11v. Since the rise is slow and the fall is fast, the time differential between the input peak and fall of the Schmidt trigger will be more consistent; therefore, the fall of the input signal is used to form the output pulse. The pulse is generated in the LC timing network and will be seen on the output terminal as a −N current mode signal of 0.6 microsecond duration.

FINAL AMPLIFIER CHECKING

The following items concerning TAU final amplifiers should be checked whenever a tape system shows write compare or read failures in excess of the engineering specifications.

1. Check the clipping levels. These should be approximately 14.5 volts for write (one continuous record), and 13.5 volts for read. These voltages can be checked at 14B4H14E for synchronization (Systems A1.40.10.1).
2. Check the output of the final amplifiers at both high and low clip. The pulse amplitude should range from 1v to −2v peak-to-peak. At the point where the pulse crosses 0 volts, the pulse width should be approximately 0.4 to 0.8 microsecond. The positive-going spike in the center of the pulse should never rise above −2v. Test points can be located on Systems A1.40.10.1. Wave shapes shown in Figure 5-17 are approximate.

5.4.2 Clipping Level Circuits

Four cards are used to establish the various clipping levels in TAU (Figure 5-16).

The basic card (WU−−) affects the clip level in both A and B channels. This circuit contains a voltage divider and a transistor switch that can be activated as needed to alter the divider output. As presently used, this switch is turned on when TAU is in not-write status, giving less clipping voltage at the output.

A second card (ABP−) is connected in parallel to the basic circuit to further control the resultant clipping voltage. This card has a number of output voltage possibilities and can be switched independently of the basic card.

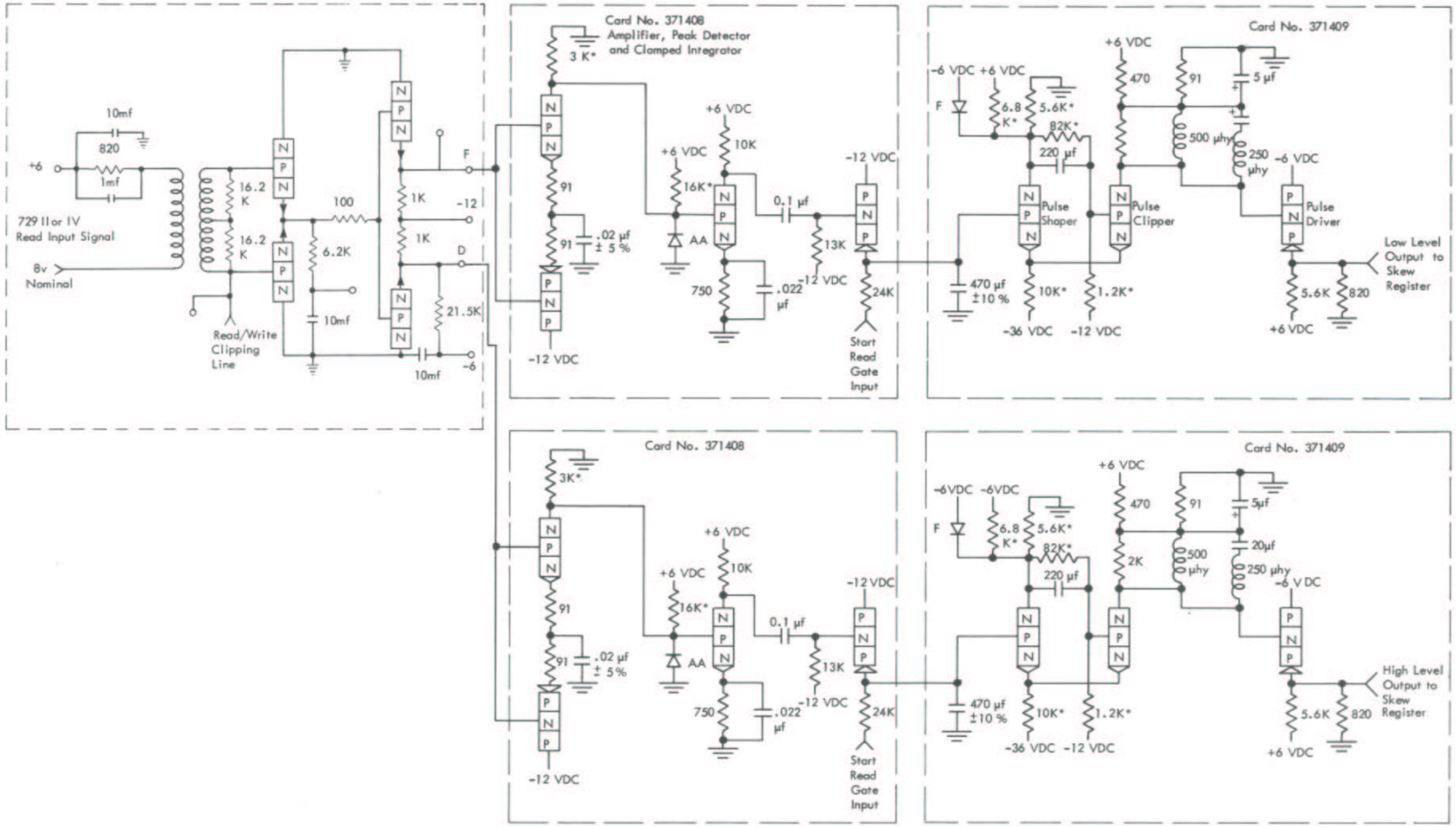
Since these cards affect both channels equally, a second set of cards is necessary to control the relationship between A and B channels.

These cards (ABQ− and ABR−) impress a positive bias on the output of the AFC− amplifier card in order to produce additional clipping on the A channel when the B channel is operating at a very high sensitivity. As in the case of the previous circuits, these cards are switched with the not-write signal.

5.4.3 P Type Trigger Circuit

Figure 5-18 shows a trigger formed by interconnecting an N and a P block. Also, located on the N block card, are a trigger delay line and a terminating load. These additional circuits allow for a choice of several output circuit configurations, as shown in Figure 5-19.

Included on the P trigger circuit schematic is a table of interconnecting card rules that apply to all circuits in TAU which utilize more than one card.



NOTES:

1. All resistor values given in ohms ± 5% and are 1/2 watt unless otherwise specified.
2. * indicates ± 1%
3. All capacitors values given in micro-farrads ± 20% unless otherwise indicated.

Figure 5-16. Sense Amplifier

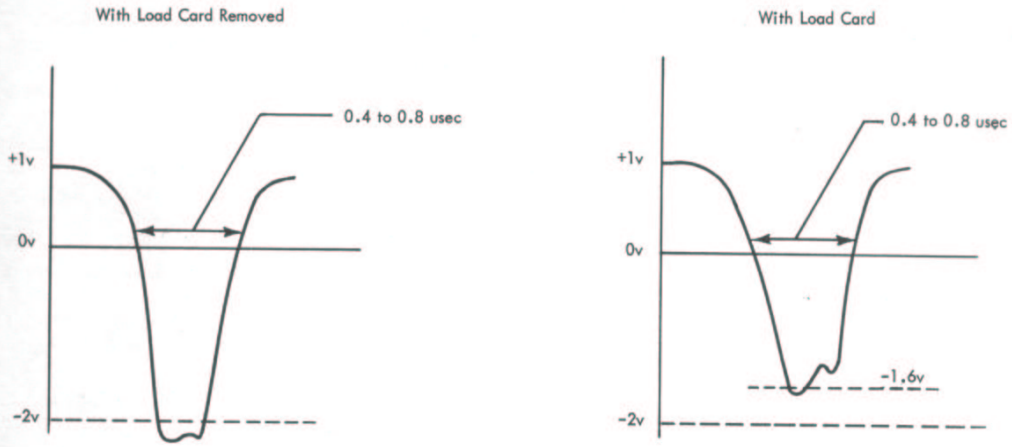
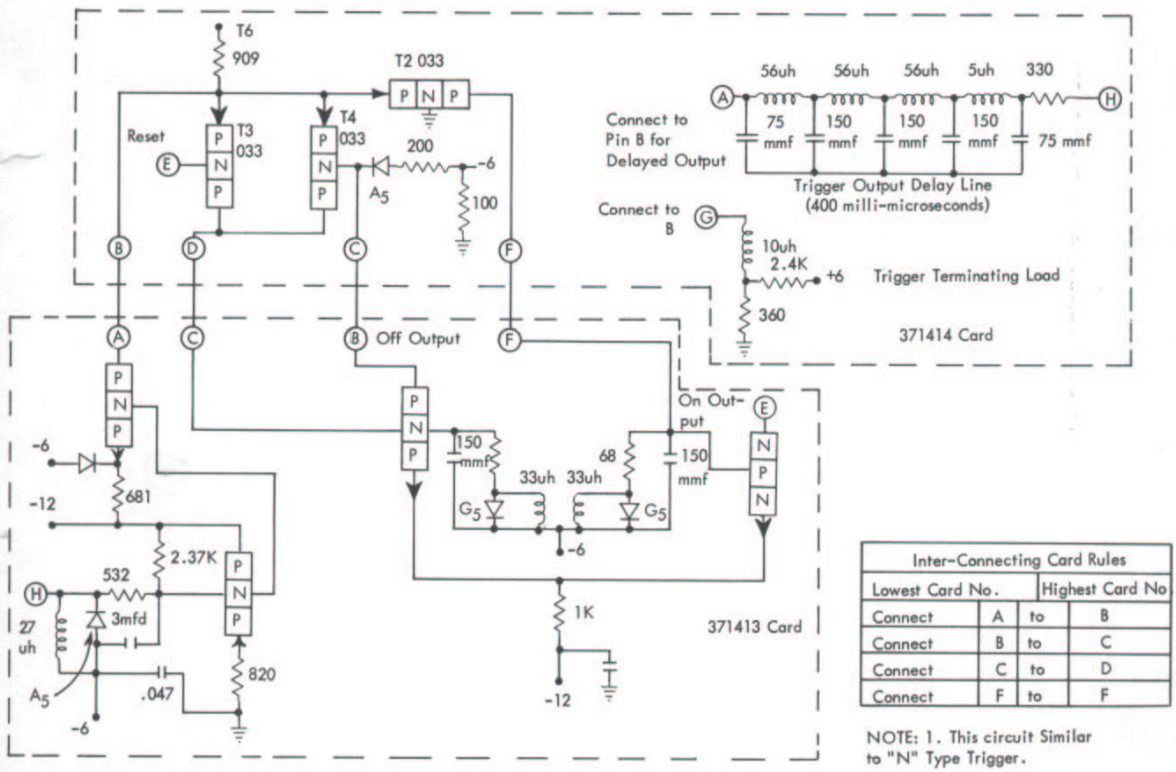


Figure 5-17. Final Amplifier Output



Inter-Connecting Card Rules			
Lowest Card No.			Highest Card No.
Connect	A	to	B
Connect	B	to	C
Connect	C	to	D
Connect	F	to	F

NOTE: 1. This circuit Similar to "N" Type Trigger.

Figure 5-18. P Type Trigger Circuit

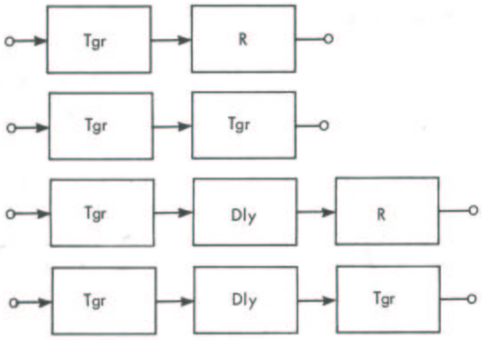


Figure 5-19. Trigger Output Configurations

5.5 Differences Between TAU I and TAU II

5.5.1 Packaging Differences

TAU I occupies three panels of one gate in a horizontal sliding gate package. TAU II occupies four panels of a vertical swinging gate package.

5.5.2 Logic Differences

TAU I contains facilities for automatically selecting proper delays and oscillator timings for the 729 II and 729 IV tape units. A separate select and ready model II line gates the proper oscillators when a 729 II tape unit on the line is selected. A second line, select and ready model IV, gates the proper oscillators when a 729 IV on the line is selected.

These lines are generated in the tape unit as the output of a relay. This relay is under direct control of two lines from TAU, *set high density* and *set low density*, and a key on the tape unit that allows the operator to select the desired density status.

The density status relay in the 729 II and IV will be reset to high density when power is applied. Logical control for the lines originates in the housekeeping portion of the program as the instructions set high density or set low density, preceded by a select tape unit. The set density control line should be held on until the correct response is received from the tape unit. This is similar to tape indicator instructions. To eliminate timing problems involving the transmission lines, the select and ready line is used along with the high-low density line to send these instructions.

Character rates and bit densities involved when using TAU I multifunction 729 tape units are:

	BIT DENSITY	CHARACTER RATE
729 II LO	200 BPI*	15K char/sec
729 II HI	556 BPI	41.7K char/sec
729 IV LO	200 BPI	22.5K char/sec
729 IV HI	556 BPI	62.5K char/sec

*BPI = Bits per inch.

TAU II does not contain the logic functions necessary to switch 729 II or IV tape units. The tape unit desired must be specified when ordering a TAU II or, if more than one combination is necessary, the additional oscillators and switching must be provided externally to TAU.

5.6 TAU Applications

TAU is used with the IBM 7090, 7070, and IBM 7080 Data Processing Systems and the 1401 series machines.

IBM
International Business Machines Corporation
112 East Post Road
White Plains, New York

Printed in U.S.A. 223-6867-2